


PRELIMINARY DATA SHEET

SDA 9415-B13
DAEDALUS
Display Processor and
Scan Rate Converter
using Embedded DRAM
Technology Units

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|------------------------------------------|---------------------------------------------------------------------------------------|
| SDA 9415 - B13 | |
| Revision History: 2000-05 (V 1.0) | |
| Previous Versions: 1999-04-01 | |
| | Changes to the previous issue Version 00, Edition 04.99, are marked with a change bar |
| 05.2000 | editorial changes only (no change of content) |
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Introduction**1 Introduction**

The SDA 9415 is a new component of the Micronas MEGAVISION[®] IC set, which enables the system to reduce large area and line flickering of interlaced TV standards.

The scan rate conversion to 100/120 Hz interlaced or 50/60 Hz progressive scan is motion vector based. For the 100/120 Hz (50/60 Hz) conversion the SDA 9415 really calculates 100/120 Hz (50/60 Hz) fields with continuous motion phases to avoid double contour effects in the motion display. In the special case of movie sources, which have a non-continuous motion phase, the SDA 9415 generates at the output an appropriate sequence with a continuous motion phase („True Motion“).

Due to the frame based signal processing, the noise reduction has been greatly improved. Furthermore different motion detectors for luminance and chrominance have been implemented. For automatic controlling of the noise reduction parameters a noise measurement algorithm is included, which measures the noise level in the picture or in the blanking period. In addition a spatial noise reduction is implemented, which reduces the noise even in the case of motion.

The SDA 9415 has two input channels, which can be used for different features like Picture-in-Picture (maximum approximately 1/9 picture) and “Double-window/Split-screen”. The two input signals can be scaled horizontally and vertically with variable factors. Panorama modes will be supported.

Besides that an algorithm for the detection of letter box pictures is included. The SDA 9415 delivers the start and the end line of the active picture part of the input signal to an external μC . The μC calculates the zoom factors for displaying the active picture part on the full screen and sends this values back to the SDA 9415.

Picture sharpness can be greatly improved by a LTI (luminance transition improvement) or/and peaking and a CTI (colour transition improvement) algorithm. The resolution of the output signals is 9 bit. The SDA 9415 has analog output signals.

Features

2 Features

- **Different application modes**
 - **SRC mode:**
 - High performance scan rate converter
 - High performance scan rate converter plus high resolution frame based joint-line-free Picture-in-Picture (maximum approximately 1/9 picture)
 - **SSC mode:**
 - Split screen applications with two signal sources (e.g. double window)
 - **MUP mode:**
 - Multipicture display mode (e.g. tuner scan)
- **8 bit amplitude resolution of each input channel**
 - Two input channels
 - Input frequency up to 27 MHz
 - ITU-R 656 data format (8 wires data only and additional sync information or 8 wires including sync information)
 - 4:2:2 luminance and chrominance parallel (2x8 wires)
- **Two different representations of input chrominance data**
 - 2's complement code
 - Positive dual code
- **Two flexible input sync controllers**
- **Vertical peaking of the input signal**
- **Flexible scaling of the input signal**
 - Flexible digital vertical compression of the input signal (1.0, ... [2 line resolution] ... , 1/32)
 - Flexible horizontal compression and expansion of the input signal (2.0, ... [4 pixel resolution] ... , 1.0 , ... [4 pixel resolution] ... , 1/32)
 - Panorama mode (programmable characteristic)
- **Noise reduction**
 - Motion adaptive spatial and temporal noise reduction (3D-NR)
 - Temporal noise reduction for luminance and chrominance, frame based or field based
 - Different motion detectors for luminance and chrominance or identical
 - Flexible programming of the temporal noise reduction parameters
 - Automatic measurement of the noise level (5 bit value, readable by I²C-bus)
- **3-D motion estimation**
 - High performance motion estimation based on block matching algorithm
 - Film mode detector (PAL and NTSC), Global motion flag (readable by I²C bus)
- **Automatic detection of letter box formats (readable by I²C bus)**
- **TV mode detection by counting line numbers (PAL, NTSC, readable by I²C bus)**
- **Embedded memory**
 - 6 Mbit embedded DRAM core for field memories
 - 1,1 Mbit embedded DRAM core for line memories, vector memory, block-to-line

Features

- converter
- 36 kbit SRAM for block matching, line-to-block converter
- **Flexible clock and synchronization concept**
 - Decoupling of the input and output clock system possible
- **Scan rate conversion**
 - Motion compensated 100/120 Hz interlaced scan conversion (Micronas VDU)
 - Motion compensated 50/60 Hz progressive scan conversion (Micronas VDU)
 - Simple interlaced modes: ABAB, AABB, AAAA, BBBB
 - Simple progressive modes: AB, AA*, B*B
 - True Motion: 50 Hz motion resolution even for 25 Hz PAL film sources
60 Hz motion resolution even for 30 Hz NTSC film sources
 - Large area and line flicker reduction
- **Flexible digital vertical expansion of the output signal (1.0, ... [1/64] ... , 2.0)**
- **Sharpness improvement**
 - Digital colour transition improvement (DCTI)
 - Digital luminance transition improvement (DLTI)
 - Peaking (luminance only)
- **Flexible output sync controller**
 - Flexible positioning of the two output channels in all application modes
 - Flexible height and width of the two output pictures
 - Flexible programming of the output sync raster
- **Signal manipulations**
 - Still frame or field
 - Insertion of coloured background
 - Insertion of a selection border
 - Adjustable delay between Y and UV signal (+4,...[1]...,-3 input pixels) at the input side
 - Adjustable delay between Y and UV signal (+3,...[0.5]...,- 4 output pixels) at the output side
- **Three D/A converters**
 - 9 bit amplitude resolution for Y, -(R-Y), -(B-Y) output
 - 60 MHz maximal clock frequency
 - Two-fold oversampling
 - Simplification of external analog post filtering and differential analog outputs
- I²C-bus control (400 kHz)
- P-MQFP-100 package
- 3.3 V ± 5% supply voltage

Block diagram

3 Block diagram

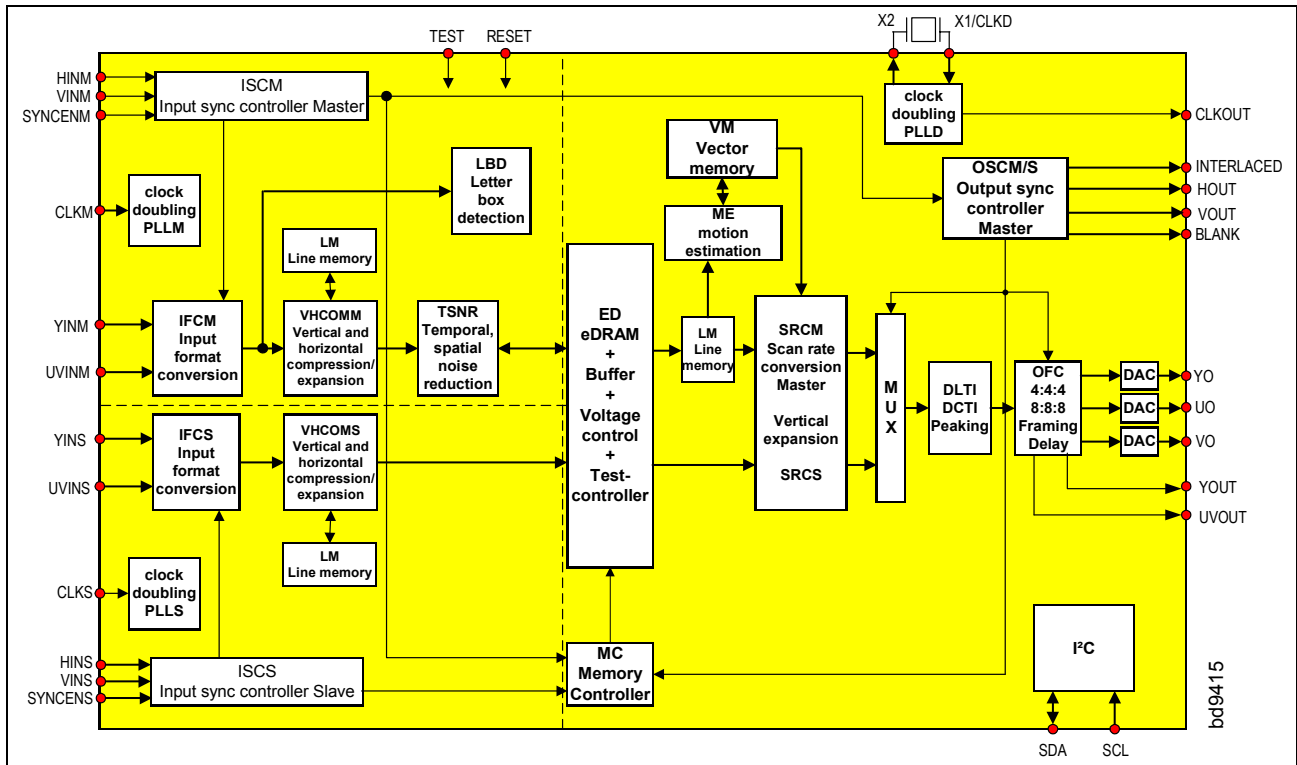


Figure 1 Block diagram

The SDA 9415 contains the blocks, which will be briefly described below:

- ISCM/S - Flexible input sync controller
- IFCM/S - Input format conversion, Adjustable delay
- VHCMM/S - Vertical and horizontal compression, horizontal expansion, panorama mode (only M)
- TSNR - Temporal and spatial noise reduction, noise measurement
- LBD - Letter box detection
- ME - Motion estimation, Film mode and phase detection
- MC - Memory controller
- OSCM/S - Flexible output sync controller
- OFC - Output format conversion, 4:4:4, 8:8:8 interpolation, Adjustable delay
- SRCM/S - Scan rate conversion, vertical expansion
- MUX - Combination of the two output channels
- DLTI/DCTI/Peaking - Luminance and chrominance transition improvement, luminance peaking
- I²C - I²C bus interface
- PLLM/S/D - PLL for frequency doubling
- LM - Line memory core, VM - Vector memory core
- ED - eDRAM core

Block diagram

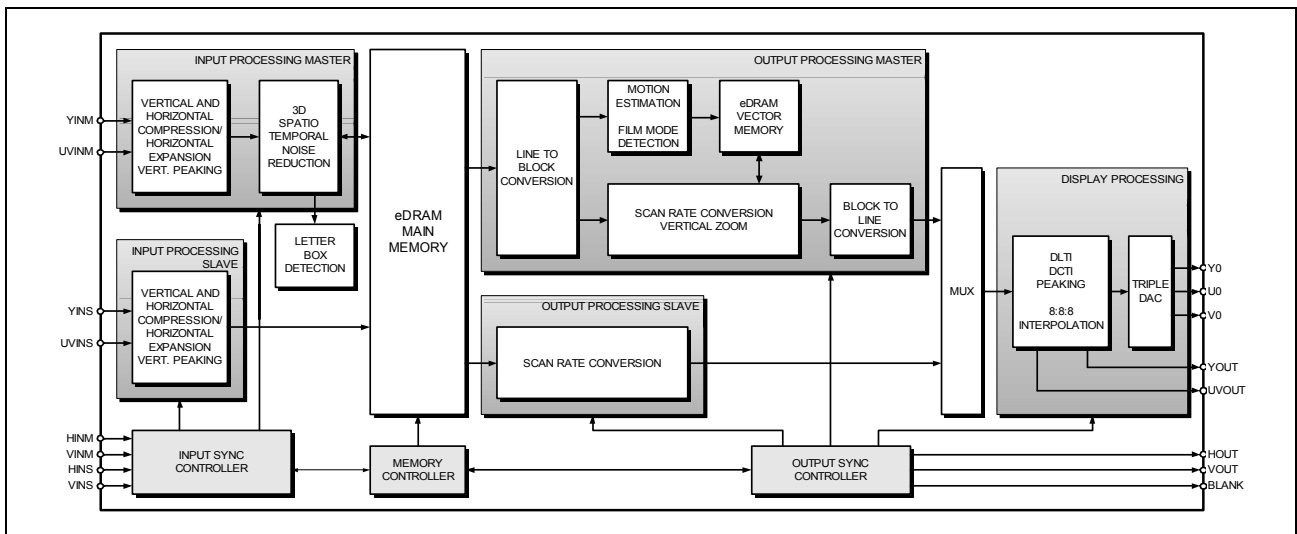


Figure 2 Block diagram 2

Pin Description

4 Pin Description

Pin Diagram: P-MQFP-144-2

(top view)

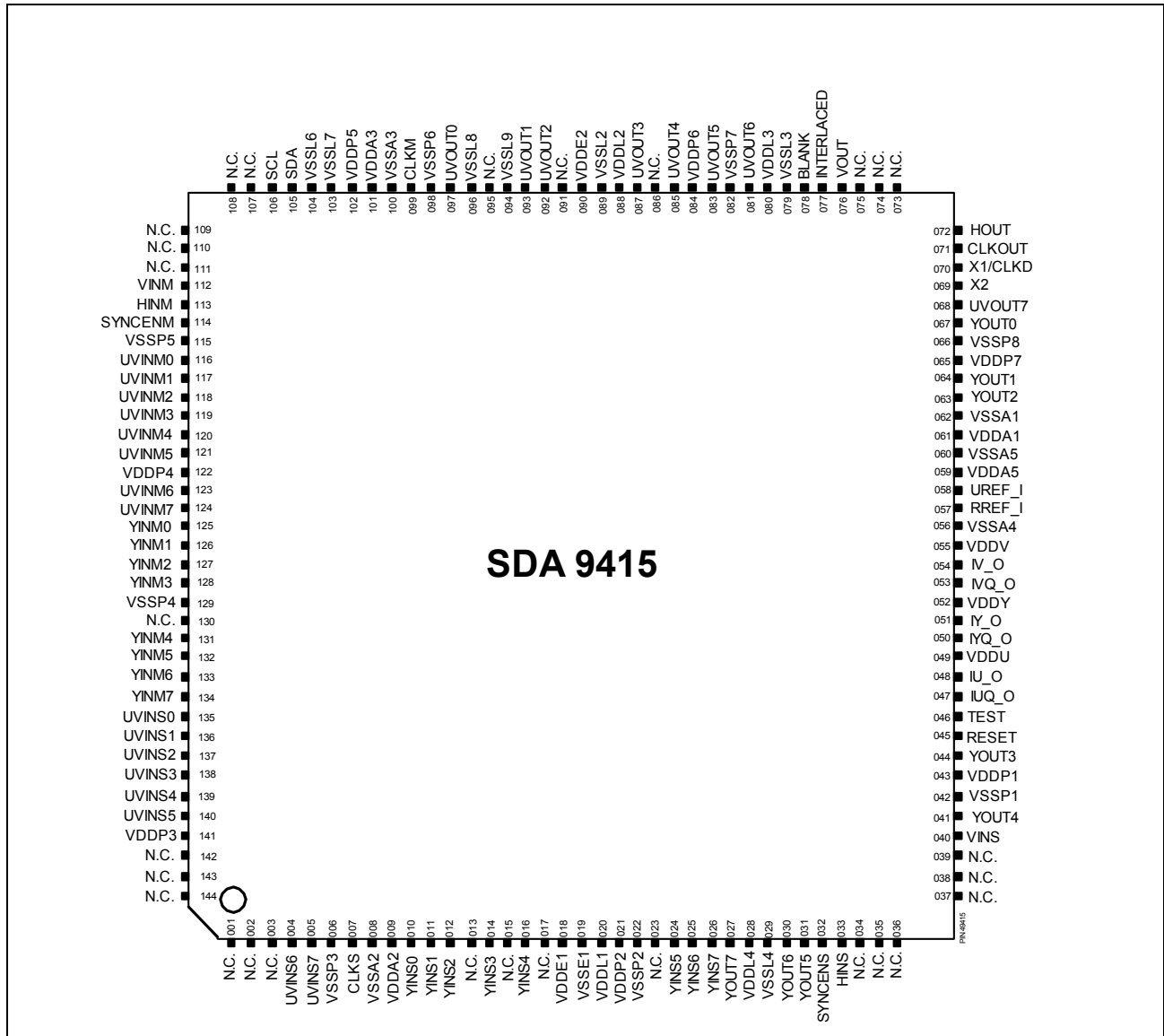


Figure 3 Pin configuration

Pin Description

Table 1 Pin definitions and functions

| Symbol | Pin Num. | Input Outp. | Function |
|-------------|----------------------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VSSLx *) | 19, 29, 79, 89, 94, 96, 103, 104 | S | Supply voltage for digital logic parts ($V_{SS} = 0\text{ V}$) |
| VDDLx | 20, 28, 80, 88, 90 | S | Supply voltage for digital logic parts ($V_{DD} = 3.3\text{ V}$) |
| VSSPx | 6, 22, 42, 66, 82, 98, 115, 129 | S | Supply voltage for pads ($V_{SS} = 0\text{ V}$) |
| VDDPx | 21, 43, 65, 84, 102, 122, 141 | S | Supply voltage for pads ($V_{DD} = 3.3\text{ V}$) |
| VSSE1 | 19 | S | Supply voltage for embedded DRAM ($V_{SS} = 0\text{ V}$) |
| VDDEx | 18, 90 | S | Supply voltage for embedded DRAM ($V_{DD} = 3.3\text{ V}$) |
| VSSAx | 8, 56, 60, 62, 100 | S | Supply voltage for analog PLL and for analog parts DAC ($V_{SS} = 0\text{ V}$) |
| VDDAx | 9, 59, 61, 101 | S | Supply voltage for analog PLL and for analog parts DAC ($V_{DD} = 3.3\text{ V}$) |
| YINM 0...7 | 125, ..., 128; 131, ..., 134 | I/TTL | Data input Y master channel |
| UVINM 0...7 | 116, ..., 121; 123; 124 | I/TTL PD | Data input UV master channel |
| YINS 0...7 | 10, ..., 12; 14; 16; 24, ..., 26 | I/TTL PD | Data input Y slave channel |
| UVINS 0...7 | 135, ..., 140; 4; 5 | I/TTL PD | Data input UV slave channel |
| RESET | 45 | I/TTL | System reset. The RESET input is low active. In order to ensure correct operation a "Power On Reset" must be performed. The RESET pulse must have a minimum duration of two clock periods of the master (CLKM) and slave clock (CLKS), respectively. |
| HINM | 113 | I/TTL PD | H-Sync input master channel |
| VINM | 112 | I/TTL PD | V-Sync input master channel |
| SYNCENM | 114 | I/TTL | Synchronization enable input master channel |
| HINS | 33 | I/TTL PD | H-Sync input slave channel |
| VINS | 40 | I/TTL PD | V-Sync input slave channel |
| SYNCENS | 32 | I/TTL | Synchronization enable input slave channel |
| SDA | 105 | IO | I ² C-Bus data line |

Pin Description

Table 1 Pin definitions and functions (continued)

| Symbol | Pin Num. | Input Outp. | Function |
|------------|---------------------------------------------------------------------------------------------------------------------------|----------------|------------------------------------------------------------------------|
| SCL | 106 | I | I ² C-Bus clock line |
| BLANK | 78 | O/TTL | Blanking signal |
| VOUT | 76 | O/TTL | V-Sync output |
| HOUT | 72 | O/TTL | H-Sync output |
| INTERLACED | 77 | O/TTL | Interlace signal for AC coupled vertical deflection |
| CLKM | 99 | I/TTL | System clock master channel |
| CLKS | 7 | I/TTL | System clock slave channel |
| X1 / CLKD | 70 | I/TTL | Crystal connection / System clock display channel |
| X2 | 69 | O/ANA | Crystal connection |
| CLKOUT | 71 | O/TTL | System clock output |
| TEST | 46 | I/TTL | Test input, connect to V_{SS} for normal operation |
| YOUT7...0 | 27;30;31;41; 44;63;64;67 | O/TTL | Digital luminance output |
| UVOUT7...0 | 68;81;83;85; 87;92;93;97 | O/TTL | Digital chrominance output |
| IY_O | 51 | O/ANA | Analog luminance output Y |
| IYQ_O | 50 | O/ANA | Differential analog Y output, connect to V_{SS} for normal operation |
| VDDY | 52 | S | Supply voltage for analog parts DAC ($V_{DD} = 3.3 \text{ V}$) |
| IU_O | 48 | O/ANA | Analog luminance output U |
| IUQ_O | 47 | O/ANA | Differential analog U output, connect to V_{SS} for normal operation |
| VDDU | 49 | S | Supply voltage for analog parts DAC ($V_{DD} = 3.3 \text{ V}$) |
| IV_O | 54 | O/ANA | Analog luminance output V |
| IVQ_O | 53 | O/ANA | Differential analog V output, connect to V_{SS} for normal operation |
| VDDV | 55 | S | Supply voltage for analog parts DAC ($V_{DD} = 3.3 \text{ V}$) |
| UREF_I | 58 | I/ANA | Analog reference voltage for DACs |
| RREF_I | 57 | | Reference resistor for DACs |
| N.C. | 1,2,3,13,15, 17,23,34,35, 36,37,38,39, 73,74,75,86, 91,95,107, 108,109, 110,111, 130,142, 143,144 | | |

S: supply, I: input, O: output, TTL: digital (TTL)

ANA: analog

PD: pull down (switched on or off depending on I²C bus parameter FORMATM, FORMATS or SLAVECON)

Pin Description

*) x - placeholder for number

Pin Description

System description

5 System description

5.1 Introduction

The SDA 9415 is the first single-chip Micronas MEGAVISION[®] feature box including scan rate conversion and the necessary field memories, a second input channel for split screen applications like picture-and-picture and digital-to-analog converters. The SDA 9415 has three application modes: the SRC (Scan Rate Conversion) mode, the SSC (Split SCreen) mode and the MUP (MULTi Picture) mode.

The two input channels of the SDA 9415 are not equivalent. One input channel is always the so called “master” channel and one input channel is always the so called “slave” channel. Both channels are combined of the output side of the SDA 9415 in the “MUX” block. The master channel is always the "synchronization" master of both channels.

In the SRC mode the SDA 9415 can be used as a high performance scan rate converter. Scan rate conversion is done by a motion compensated algorithm known as Micronas VDU (Vector Driven Up conversion). In addition a high resolution frame based joint-line-free picture-and-picture (maximum approximately 1/9 picture) can be displayed. The figure below shows an example of the SRC mode.



Figure 4 Principles of SRC mode

System description

For this usage the 6 Mbit eDRAM core is separated in two luminance fields and two chrominance fields (either 4:2:0 or 4:1:1) and a memory area for luminance and chrominance fields (4:1:1) [maximum circa 1/9 picture] for picture-in-picture applications. The vector based scan rate conversion is possible for the master channel only.

For the SSC mode the 6 Mbit eDRAM core is split in two 3 Mbit areas, which are able to contain a maximum of two luminance fields and two chrominance fields (either 4:2:0 or 4:1:1). The figure below shows different applications (“Double window”, “Zoom-in-zoom-out”). In this case only a simple scan rate conversion (e.g. field doubling for interlaced conversion: AABB) for both output channels is possible.



Figure 5 Principles of SSC mode

System description

The MUP mode allows the combination of one live picture and a configuration of still pictures. The figure below shows an application. In this case only a simple scan rate conversion (e.g. field doubling for interlaced conversion: AABB or AAAA) is possible.

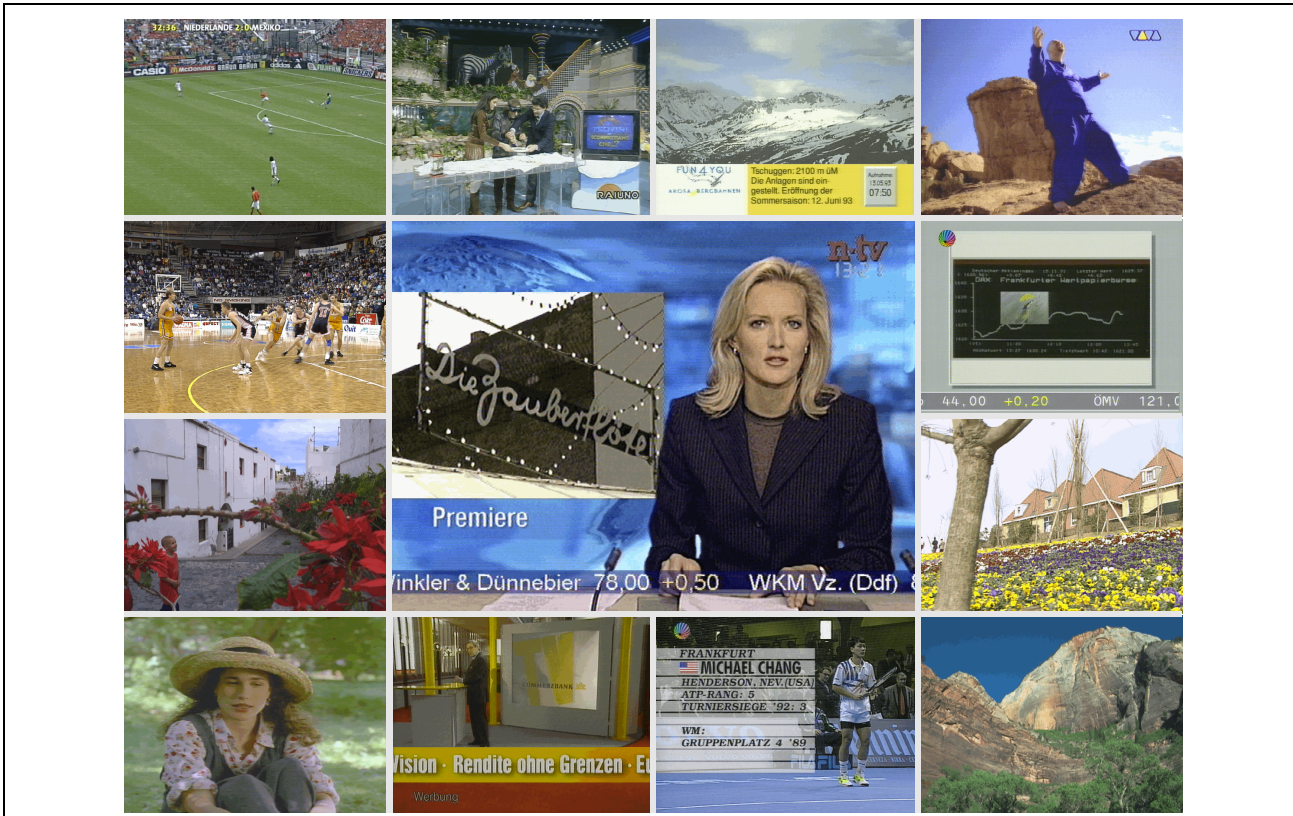


Figure 6 Principles of MUP mode

The behaviour of the master and the slave channel does not differ in general. Therefore for further description of the master and the slave channel the figures are also valid for both unless it is pointed out.

System description

5.2 Input sync controller (ISCM/ISCS)

| Signals | Pin number | Description |
|---------|------------|-----------------------------------------------------------------------------------------------------------------------------|
| HINM | 27 | horizontal synchronization signal (polarity programmable, I ² C Bus parameter 11h HINPOLM, default: high active) |
| VINM | 26 | vertical synchronization signal (polarity programmable, I ² C Bus parameter 11h VINPOLM, default: high active) |
| SYNCENM | 28 | enable signal for HINM and VINM signal, low active (" Input format conversion (IFCM/IFCS) " on page 30) |
| HINS | 77 | horizontal synchronization signal (polarity programmable, I ² C Bus parameter 33h HINPOLS, default: high active) |
| VINS | 78 | vertical synchronization signal (polarity programmable, I ² C Bus parameter 33h VINPOLS, default: high active) |
| SYNCENS | 76 | enable signal for HINS and VINS signal, low active (" Input format conversion (IFCM/IFCS) " on page 30) |

Table 2 Input signals

The input sync controller derives framing signals from the H- and V-Sync for the input data processing. The framing signals depend on different I²C Bus parameters and mark the active picture area.

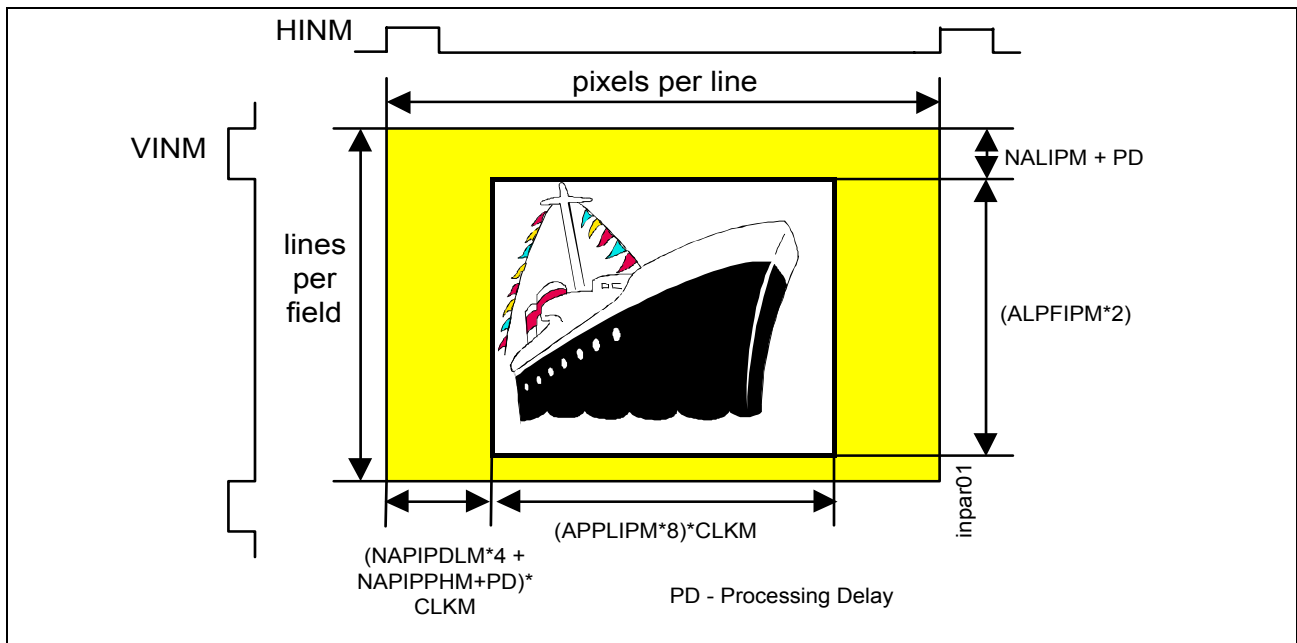


Figure 7 Input I²C Bus parameter

The distance between the incoming H-syncs in system clocks of CLKM/CLKS must be even.

System description

| I ² C Bus parameter [Default value] | Sub address | Description |
|---------------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NALIPM [20] | 12h | Not Active Line InPut Master defines the number of lines from the V-Sync to the first active line of the field |
| NALIPS [20] | 34h | Not Active Line InPut Slave defines the number of lines from the V-Sync to the first active line of the field |
| ALPFIPM [144] | 10h | Active Lines Per Field InPut Master defines the number of active lines |
| ALPFIPS [144] | 32h | Active Lines Per Field InPut Slave defines the number of active lines |
| NAPLIPM NAPIPDLM [0] NAPIPPHM [0] | 03h, 0Ch | Not Active Pixels Per Line InPut Master defines the number of pixels from the H-Sync to the first active pixel of the line. The number of pixels is a combination of NAPIPDLM and NAPIPPHM. |
| NAPLIPS NAPIPDLS [0] NAPIPPHS [0] | 2Dh, 2Eh | Not Active Pixels Per Line InPut defines the number of pixels from the H-Sync to the first active pixel of the line. The number of pixels is a combination of NAPIPDLS and NAPIPPHS. |
| APPLIPM [180] | 0Fh | Active Pixels Per Line InPut Master defines the number of active pixels |
| APPLIPS [180] | 31h | Active Pixels Per Line InPut Slave defines the number of active pixels |

Table 3 Input write I²C Bus parameter

Inside of the SDA 9415 a field detection block is necessary for the detection of an odd (A) or even (B) field. Therefore the incoming H-Sync H1 (delayed HINM/HINS signal, delay depends on NAPIPDLM/NAPIPDLS and NAPIPPHM/NAPIPPHS) is doubled (H2 signal). Depending on the phase position of the rising edge of the VINM/VINS signal an A (rising edge between H1 and H2) or B (rising edge between H2 and H1) field is detected. For proper operation of the field detection block, the VINM/VINS must be delayed depending on the delay of the HINM/HINS signal (H1). The figure below explains the field detection process and the functionality of the VINDELM/VINDELS I²C Bus parameter (inside the SDA 9415 the delayed VINM/VINS signal is called Vd and the detected field signal is called Ffd).

System description

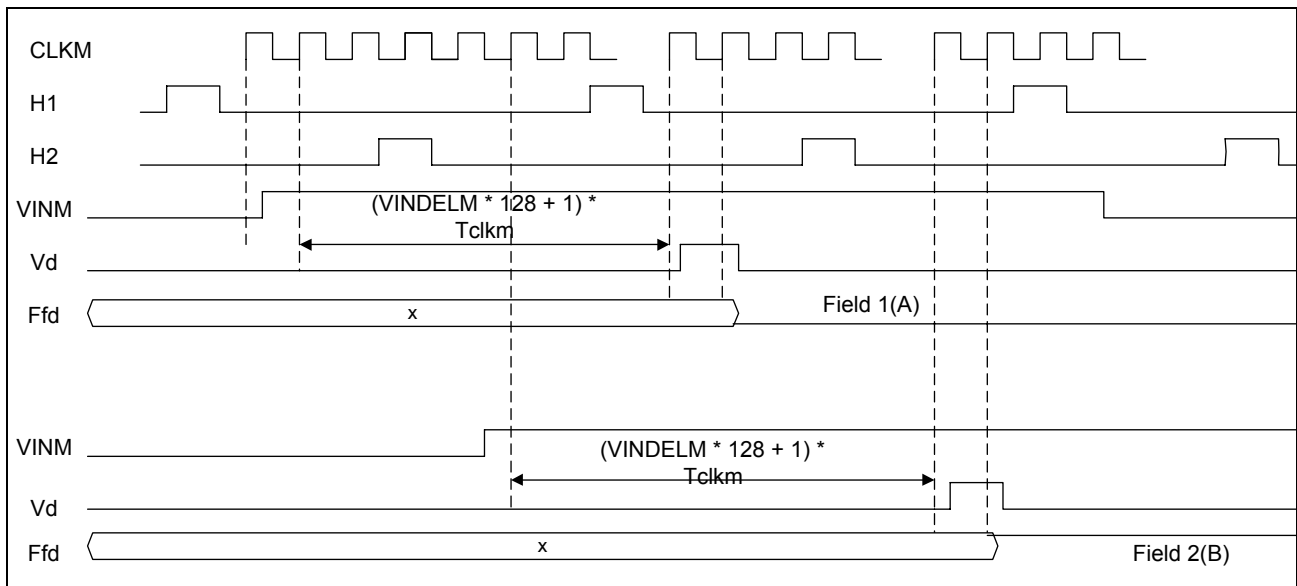


Figure 8 Field detection and VINM delay

| I ² C Bus parameter [Default value] | Sub address | Description |
|---------------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VINDELM [0] | 11h | Delay of the incoming V-Sync VINM (must be adjusted depending on the delay of the HINM signal) |
| VINDELS [0] | 33h | Delay of the incoming V-Sync VINS (must be adjusted depending on the delay of the HINS signal) |
| FIINVM 1 : Field A=1 [0]: Field A=0 | 0Bh | Inversion of the internal field polarity master |
| FIINVS 1 : Field A=1 [0]: Field A=0 | 2Dh | Inversion of the internal field polarity slave |
| VCRMDEM [1]: on 0 : off | 0Bh | In case of non standard interlaced signals (VCR, Play-Stations) a filtering of the internal field signal has to be done (should also be used for normal TV signals) |
| VCRMDES [1]: on 0 : off | 2Dh | In case of non standard interlaced signals (VCR, Play-Stations) a filtering of the internal field signal has to be done (should also be used for normal TV signals) |

Table 4 Input write I²C Bus parameter

In case of non-standard signals the field order is indeterminate (e.g. AAA... , BBB... , AAABAAAB..., etc.). Therefore a special filtering algorithm is implemented, which can be switched on by the I²C Bus parameter VCRMDEM/VCRMDES. It is recommended to set the I²C Bus parameter VCRMDEM=1. In other case (VCRMDEM=0) an additional

System description

internal signal VTSEQM is generated. This signal level is high (VTSEQM=1), if at least the last to fields were identical. Due to the fixed storage places of the fields in the internal memory block, this information is necessary for the scan rate conversion processing ("**Output sync controller (OSCM/S)**" on page 81, it is recommended in case of VCRMODEM=0 to choose an adaptive operation mode).

The OPDELM I²C Bus parameter is used to adjust the outgoing V-Sync VOUT in relation to the incoming delayed V-Sync VINM. In case of SSC and MUP mode the recommended default value should not be changed.

| I ² C Bus parameter [Default value] | Sub address | Description |
|---------------------------------------------------|-------------|------------------------------------------------------------------------------------------------|
| OPDELM [170] | 1Bh | Delay (in number of lines) of the internal V-Sync (delayed VINM) to the outgoing V-Sync (VOUT) |

Table 5 Input write I²C Bus parameter

The internal line counter is used to determine the information about the standard of the incoming signal.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|-----------------------------------------------------------------|
| TVMODEM | 7Bh | TV standard of the incoming signal master: 1: NTSC 0: PAL |
| TVMODES | 7Dh | TV standard of the incoming signal slave: 1: NTSC 0: PAL |

Table 6 Input read I²C Bus parameter

System description

5.3 Input format conversion (IFCM/IFCS)

| Signals | Pin number | Description |
|------------|-------------------------|--------------------------|
| YINM0...7 | 39,40,41,42,44,45,46,47 | luminance input master |
| UVINM0...7 | 30,31,32,33,34,35,37,38 | chrominance input master |
| YINS0...7 | 61,62,63,64,65,71,72,73 | luminance input slave |
| UVINS0...7 | 48,49,50,51,52,53,55,56 | chrominance input slave |

Table 7 Input signals

The SDA 9415 accepts at the input side the sample frequency relations of Y : (B-Y) : (R-Y): 4:2:2 and CCIR 656.

| Data Pin | CCIR 656 FORMATM = 1X FORMATM = 01 | | | | 4:2:2 Parallel FORMATM = 00 | |
|----------|------------------------------------------|-----------------|-----------------|-----------------|--------------------------------|-----------------|
| | U ₀₇ | Y ₀₇ | V ₀₇ | Y ₁₇ | Y ₀₇ | Y ₁₇ |
| YINM7 | U ₀₇ | Y ₀₇ | V ₀₇ | Y ₁₇ | Y ₀₇ | Y ₁₇ |
| YINM6 | U ₀₆ | Y ₀₆ | V ₀₆ | Y ₁₆ | Y ₀₆ | Y ₁₆ |
| YINM5 | U ₀₅ | Y ₀₅ | V ₀₅ | Y ₁₅ | Y ₀₅ | Y ₁₅ |
| YINM4 | U ₀₄ | Y ₀₄ | V ₀₄ | Y ₁₄ | Y ₀₄ | Y ₁₄ |
| YINM3 | U ₀₃ | Y ₀₃ | V ₀₃ | Y ₁₃ | Y ₀₃ | Y ₁₃ |
| YINM2 | U ₀₂ | Y ₀₂ | V ₀₂ | Y ₁₂ | Y ₀₂ | Y ₁₂ |
| YINM1 | U ₀₁ | Y ₀₁ | V ₀₁ | Y ₁₁ | Y ₀₁ | Y ₁₁ |
| YINM0 | U ₀₀ | Y ₀₀ | V ₀₀ | Y ₁₀ | Y ₀₀ | Y ₁₀ |
| UVINM7 | | | | | U ₀₇ | V ₀₇ |
| UVINM6 | | | | | U ₀₆ | V ₀₆ |
| UVINM5 | | | | | U ₀₅ | V ₀₅ |
| UVINM4 | | | | | U ₀₄ | V ₀₄ |
| UVINM3 | | | | | U ₀₃ | V ₀₃ |
| UVINM2 | | | | | U ₀₂ | V ₀₂ |
| UVINM1 | | | | | U ₀₁ | V ₀₁ |
| UVINM0 | | | | | U ₀₀ | V ₀₀ |

Table 8 Input data formats

X_{ab}: X: signal component a: sample number b: bit number

System description

In case of CCIR 656 three modes are supported (FORMATM/FORMATS=11 means full CCIR 656 support, including H-, V-Sync and Field signal, FORMATM/FORMATS=01 means only data processing, H- and V-Sync have to be added separately according PAL/NTSC norm, FORMATM/FORMATS=10 means only data processing, H- and V-sync have to be added separately according CCIR656-PAL/NTSC norm). The representation of the samples of the chrominance signal is programmable as positive dual code (unsigned, I²C Bus parameter TWOINM/TWOINS=0) or two's complement code (TWOINM/TWOINS=1, "**I²C Bus**" on page 123, I²C Bus parameter 0Bh,2Dh). Inside the SDA 9415 all algorithms assume positive dual code.

| FORMATM/ FORMATS | HINS/HINS | VINM/VINS | YINM/YINS | UVINM/UVINS |
|-------------------------|-----------|-----------|-----------|-------------|
| 00 | PAL/NTSC | PAL/NTSC | 4:2:2 | 4:2:2 |
| 01 (CCIR 656 only data) | PAL/NTSC | PAL/NTSC | CCIR 656 | x |
| 10 | CCIR 656 | CCIR 656 | CCIR 656 | x |
| 11 (full CCIR 656) | x | x | CCIR 656 | x |

Table 9 Input sync formats

The amplitude resolution for each input signal component is 8 bit, the maximum clock frequency is 27 MHz. Consequently the SDA 9415 is dedicated for application in high quality digital video systems.

System description

The **Figure 9** shows the generation of the internal H- and V-syncs in case of full CCIR 656 mode. The H656 sync is generated after the EAV. The V656 and F656 signals change synchronously with the EAV timing reference code.

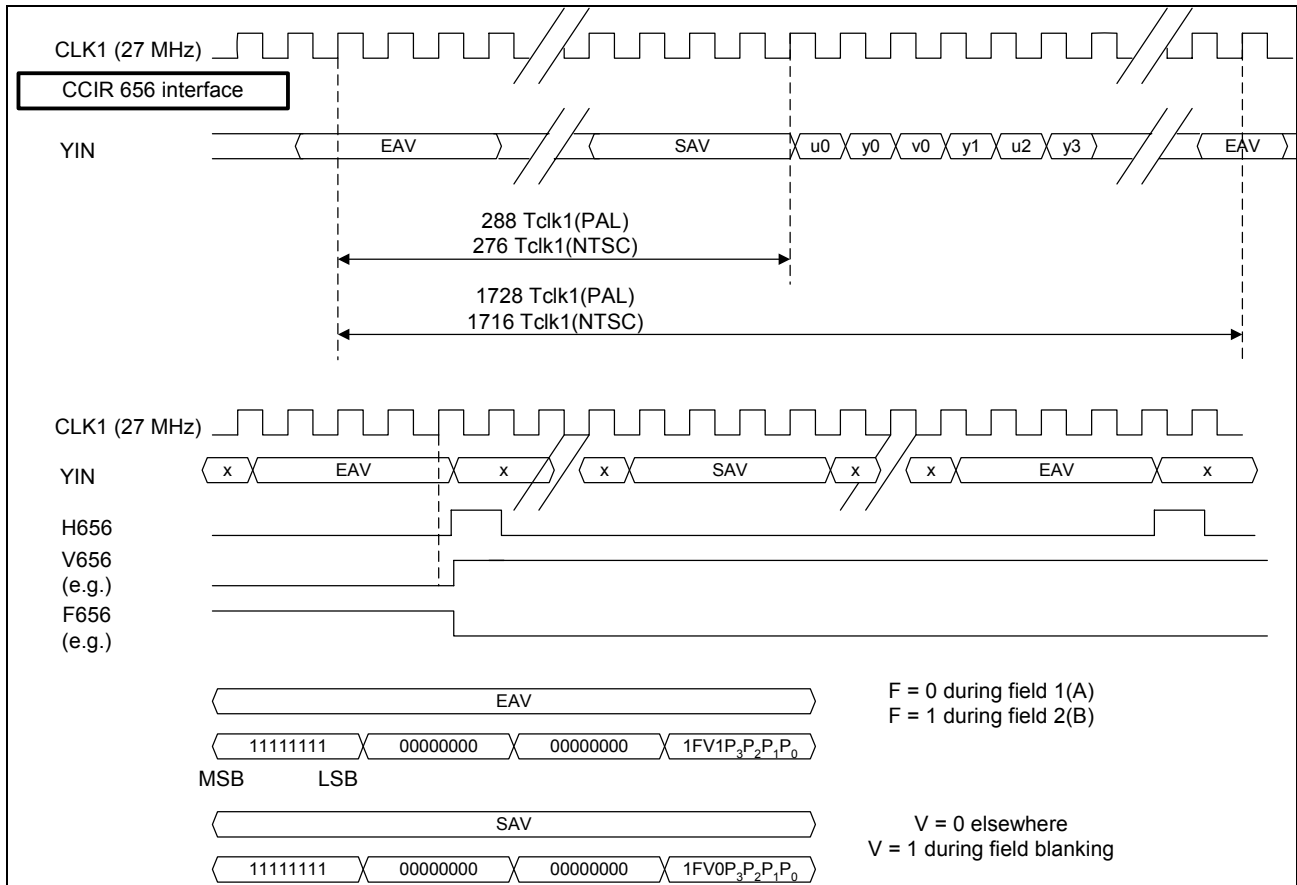


Figure 9 Explanation of 656 format

The **Figure 10** explains the functionality of the SYNCENM/SYNCENS signal. The SDA 9415 needs the SYNCENM/SYNCENS (synchronization enable) signal, which is used to gate the YINM/YINS, UVINM/UVINS as well as the HINM/HINS and the VINM/VINS signal. This is implemented for frontends which are working with 13.5 MHz and a large output delay time for YINM/YINS, UVINM/UVINS, HINM/HINS and VINM/VINS (e.g. Micronas VPC32XX, output delay: 35 ns). For this application the half system clock CLKM/CLKS (13.5 MHz) from the frontend should be provided at this pin. In case the frontend is working at 27.0 MHz with sync signals having delay times smaller than 25 ns, this input can be set to low level (SYNCENM/SYNCENS= V_{SS}) (e.g. Micronas SDA 9206, output delay: 25 ns). Thus the signals YINM/YINS, UVINM/UVINS, HINM/HINS and VINM/VINS are sampled with the CLKM/CLKS system clock when the SYNCENM/SYNCENS input is low.

The **Figure 10** shows the gated inputs signals YINMen, UVINMen, HINMen and VINMen.

System description

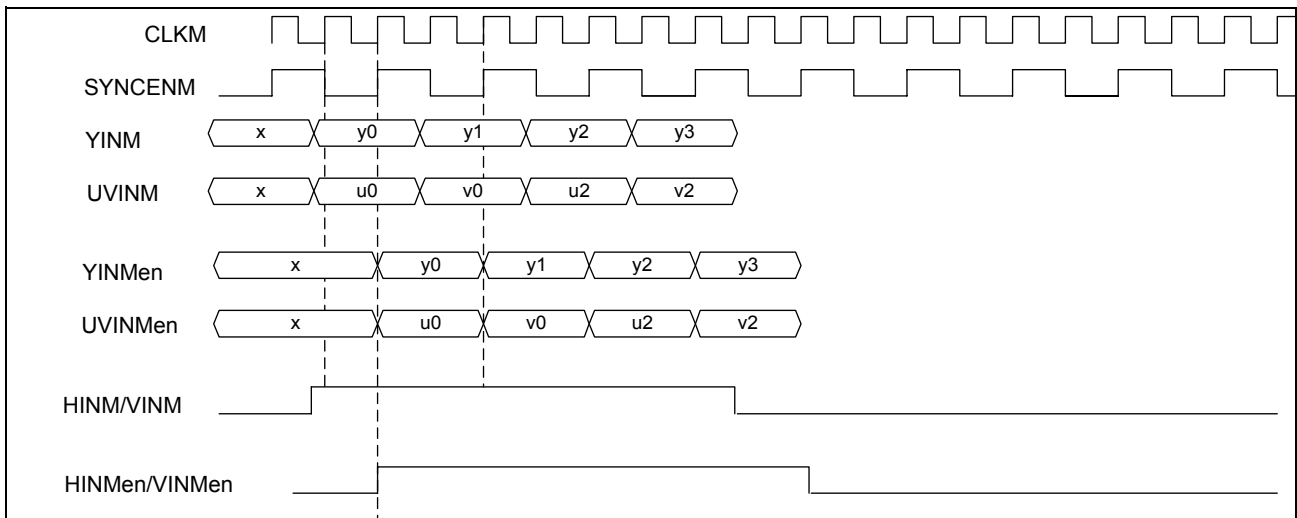


Figure 10 SYNCENM/SYNCENS signal

The Figure 11 shows the input timing and the functionality of the NAPIPDLM/NAPIPDLS and NAPIPPHM/NAPIPPHS I²C Bus parameter in case of CCIR 656 and 4:2:2 parallel data input format for one example. The signals HINMint, YINMint and UVMint are the internal available sampled input signals.

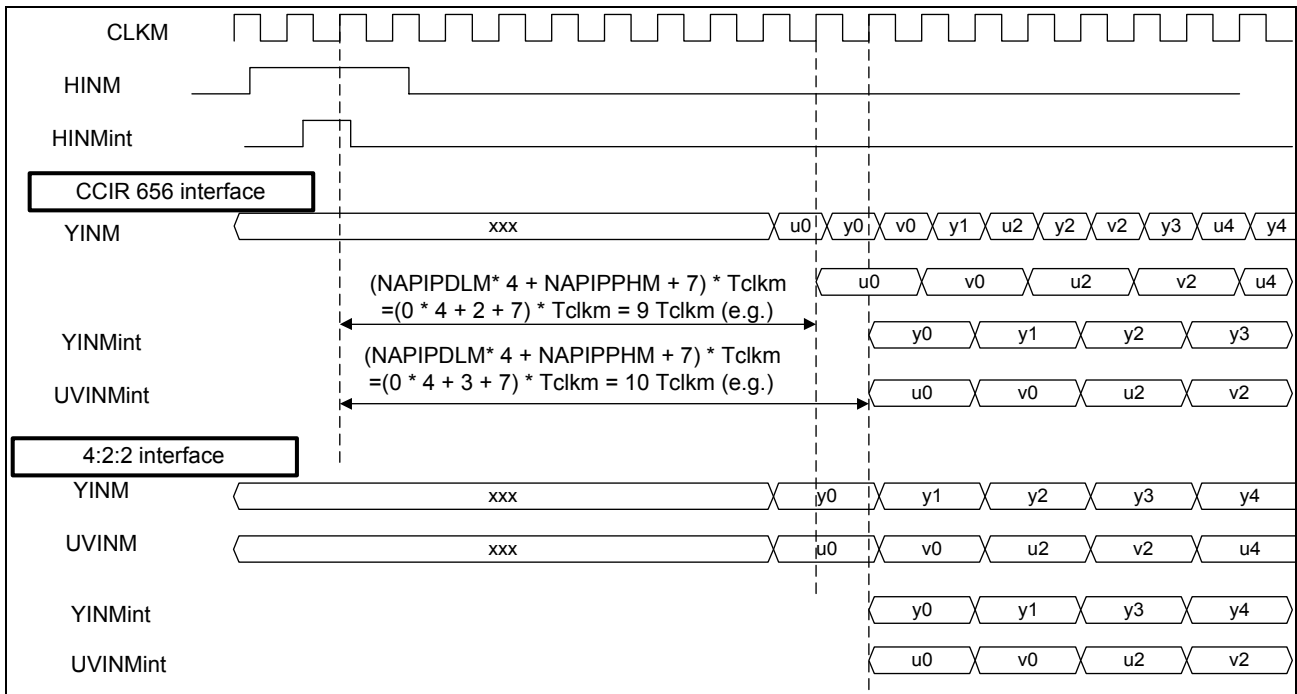


Figure 11 Input timing

System description

5.4 Input signal processing

The **Figure 12** shows a detailed block diagram of the input processing blocks. The input signal can be vertically and horizontally compressed or horizontally expanded by a large number of factors. Furthermore the input signal can be processed by different noise reduction algorithms to reduce the noise in the signal. The noise measurement block determines the noise level of the input signal. The letter box detection block finds the start and end line of letter box pictures. The information can be used by a μ C to calculate zooming factors and to control the IC for resizing the picture for a full screen display on 16:9 tubes.

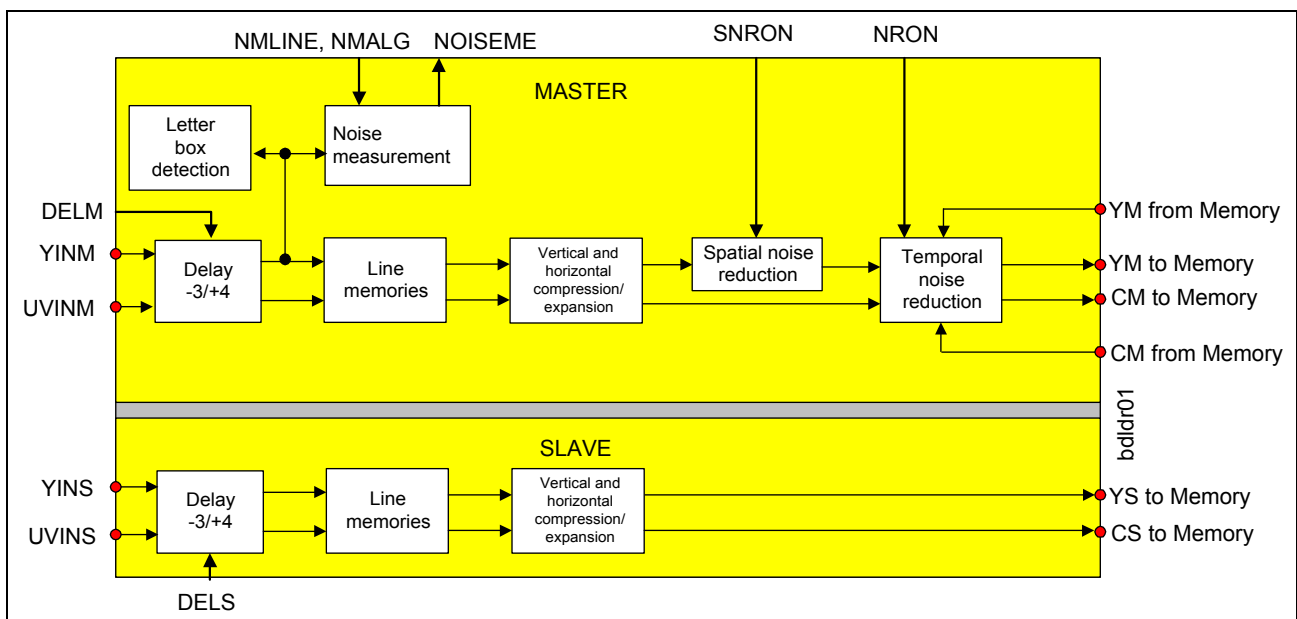


Figure 12 Block diagram of input processing blocks

The different blocks and the corresponding I²C Bus parameters will be described now in more detail.

System description
5.4.1 Adjustable delay

It is possible to adjust the luminance signal in relation to the chrominance signal in (CLKM/CLKS) steps. For further processing it is important, that the luminance signal and the chrominance signal are adjusted. Adjustment may be necessary, if the luminance and chrominance signal generated by the frontend processor are not adjusted.

| DELM/DELS (04h,026h) | Delay between luminance and chrominance data in steps of 27.0 MHz (CLKM/CLKS) |
|----------------------|-------------------------------------------------------------------------------|
| 0 | -3 |
| 1 | -2 |
| 2 | -1 |
| 3 | 0 |
| 4 | +1 |
| 5 | +2 |
| 6 | +3 |
| 7 | +4 |

Table 10 DELM/DELS I²C Bus parameter

System description

5.4.2 Vertical and horizontal compression (VHCOMM/VHCOMS)

The **Figure 13** shows the block diagram of the VHCOMM and VHCOMS block. The VHCOMM and VHCOMS block are able to compress the picture in horizontal and vertical direction continuously. The minimal step size in vertical direction is two lines, the minimal step size in horizontal direction is four pixels. The figure below shows also the functionality and the formula, which shows the relation between the number of input lines (pixels) and output lines (pixels). In horizontal direction an expansion is also possible. Panorama mode in horizontal direction will be supported.

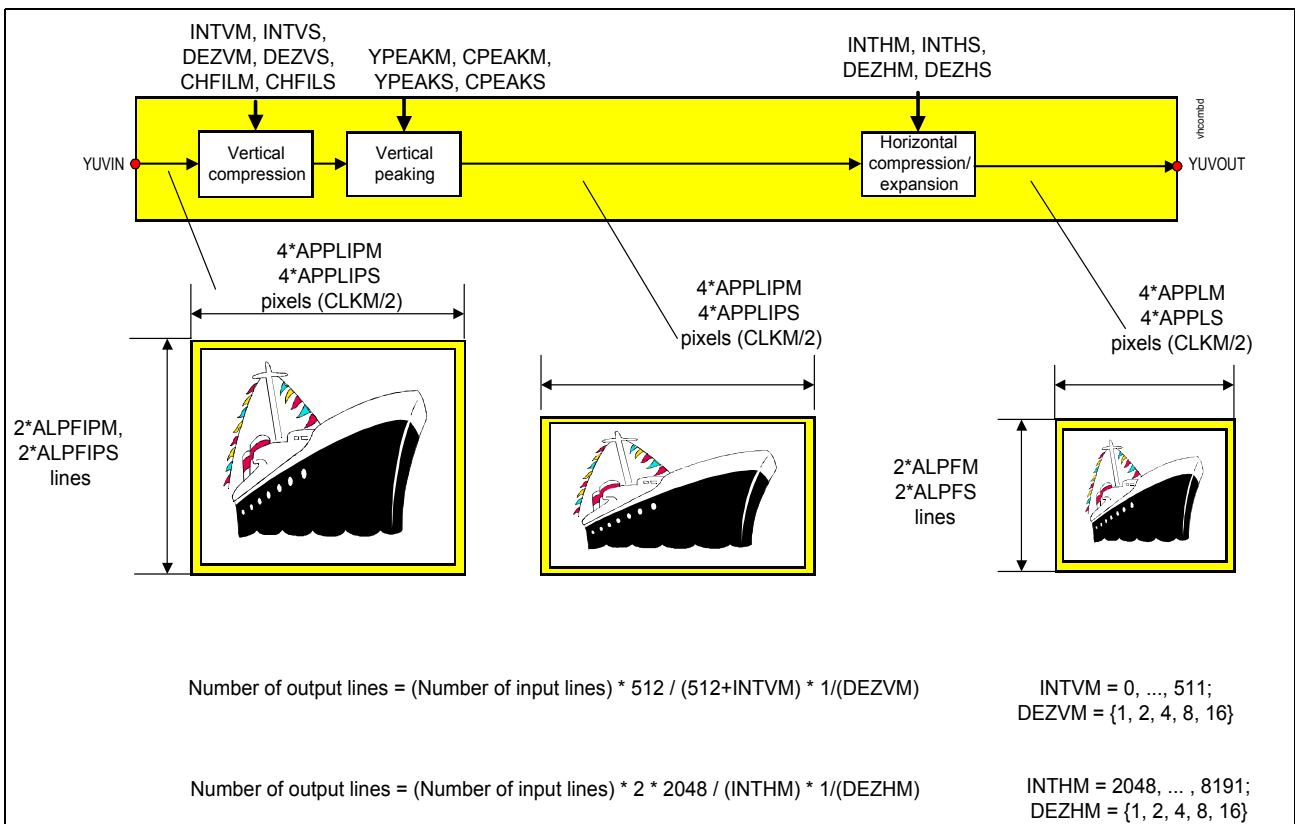


Figure 13 Block diagram of VHCOMM/VHCOMS

System description
5.4.2.1 Vertical compression and peaking

The overall reduction of the vertical compression block can be calculated by the formula:

$$\frac{512}{(512 + INTVM)} \frac{1}{DEZVM}$$

The user must specify the vertical input picture size (defined by I²C Bus parameter ALPFIPM/ALPFIPS) and the vertical output picture size (defined by I²C Bus parameter APPLM/APPLS) as well as the I²C Bus parameter INTVM/INTVS (I²C Bus parameter, 09h,0Ah,2Bh,2Ch) and DEZVM/DEZVS (I²C Bus parameter, 0Ah,2Ch), which can be calculated with the algorithm listed below (C-code).

intV, dezV: variables

```
for( intV=2*ALPFM/S, dezV=1; intV<=2*ALPFIPM/S; intV*=2, dezV*=2 )
```

```
;
```

```
intV = ((512*2*ALPFIPM/S*2+intV/2)/intV);
```

```
dezV/=2;
```

```
if(dezV>16)
```

```
{
```

```
intV=intV*dezV/16;
```

```
dezV=16;
```

```
}
```

```
INTVM/S=intV-512;
```

System description

| Vertical line size 2*ALPFM/S (2*ALPFIPM/S=288) | INTVM/S | dezV/DEZVM/S | Comment |
|------------------------------------------------------|---------|--------------|------------------------------------------------|
| 288 | 0 | 1/1 | largest size, bypass recommended DEZVM/DEZVS=0 |
| 216 | 171 | 1/1 | |
| 192 | 256 | 1/1 | Double window |
| 145 | 505 | 1/1 | |
| 144 | 0 | 2/4 | |
| 96 | 256 | 2/4 | PIP (1/3 picture) |
| 73 | 497 | 2/4 | |
| 72 | 0 | 4/5 | |
| 36 | 0 | 8/6 | |
| 18 | 0 | 16/7 | |
| 10 | 409 | 16/7 | smallest size |

Table 11 Examples of vertical filter adjustment

| dezV | DEZVM / DEZVS |
|------|---------------|
| 16 | 111 |
| 8 | 110 |
| 4 | 101 |
| 2 | 100 |
| 1 | 001 |

Table 12 Conversion table between dezV and DEZVM / DEZVS

The vertical compression block can be switched off by setting DEZVM/DEZVS equal “0” and INTVM/INTVS=0. In this case it is possible to switch on a low pass filter for the chrominance data path by the I²C Bus parameter CHFILM/CHFILS (I²C Bus parameter, 03h, 25h). If CHFILM/CHFILS is equal to “0” or “2” the vertical filter for the chrominance is switched off. If CHFILM/CHFILS is equal to “1” or “3” the vertical filter for the chrominance is switched on (**Table 17 "Input write I²C Bus parameter CHFILM/CHFILS" on page 42**).

In addition a vertical peaking of the input signal is possible.

System description

| I ² C Bus parameter | 0 (minimum value) | 3 (maximum value) |
|--------------------------------|-------------------|------------------------|
| YPEAKM/YPEAKS | peaking off | maximum peaking factor |
| CPEAKM/CPEAKS | peaking off | maximum peaking factor |

Table 13 Input write I²C Bus parameter YPEAKM/YPEAKS/CPEAKM/CPEAKS

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|--------------------------------------------------------------------|
| INTVM | 09h,0Ah | Interpolation factor for vertical compression master |
| DEZVM | 0Ah | Decimation factor for vertical compression master |
| INTVS | 2Bh,2Ch | Interpolation factor for vertical compression slave |
| DEZVS | 2Ch | Decimation factor for vertical compression master |
| YPEAKM | 0Ah | Vertical peaking factor for luminance signal master |
| CPEAKM | 0Ah | Vertical peaking factor for chrominance signal master |
| YPEAKS | 2Ch | Vertical peaking factor for luminance signal slave |
| CPEAKS | 2Ch | Vertical peaking factor for chrominance signal slave |
| ALPFM | 0Dh | Number of active lines per field after vertical compression master |
| ALPFS | 2Fh | Number of active lines per field after vertical compression slave |
| CHFILM | 03h | Chrominance filter master channel on/off |
| CHFILS | 25h | Chrominance filter slave channel on/off |

Table 14 Input write I²C Bus parameter

System description
5.4.2.2 Horizontal compression/expansion and panorama mode

The overall reduction of the horizontal compression block can be calculated by the formula:

$$2 \frac{2048}{INTHM} \frac{1}{DEZHM}$$

The user must specify the horizontal input picture size (defined by the I²C Bus parameter APPLIPM/APPLIPS) and the horizontal output picture size (defined by the I²C Bus parameter APPLM/APPLS) as well as the I²C Bus parameter INTHM/INTHS (I²C Bus parameter, 07h, 08h, 29h, 2Ah) and DEZHM/DEZHS (I²C Bus parameter, 08h, 2Ah), which can be calculated with the algorithm listed below (C-code).

intV, dezV: variables

```
for( intH=4*APPLM/S, dezH=1; intH<=4*APPLIPM/S; intH*=2, dezH*=2 )
```

```
;
```

```
intH = ((2048*4*APPLIPM/S*2+intH/2)/intH);
```

```
if( dezH>16)
```

```
{
```

```
intH= intH*dezH/16;
```

```
dezH=16;
```

```
}
```

```
INTHM/S = intH
```


System description

| Horizontal pixel size (related to CLKM/2) 4*APPLM (4*APPLIPM=720) | intH | dezH/ DEZHM/S | Comment |
|----------------------------------------------------------------------------|------|------------------|---------------------------------------|
| 1440 | 2048 | 1/1 | largest size, only 720 will be stored |
| 724 | 4073 | 1/1 | largest size, only 720 will be stored |
| 720 | 2048 | 2/4 | bypass recommended DEZHM/DEZHS=0 |
| 540 | 2731 | 2/4 | 4:3 picture on 16:9 tube |
| 364 | 4050 | 2/4 | |
| 360 | 2048 | 4/5 | Double window |
| 184 | 4007 | 4/5 | |
| 180 | 2048 | 8/6 | |
| 92 | 4007 | 8/6 | |
| 90 | 2048 | 16/7 | |
| 48 | 3840 | 16/7 | |
| 24 | 7680 | 16/7 | smallest size |

Table 15 Examples of horizontal filter adjustment

| dezH | DEZHM/S |
|------|---------|
| 16 | 111 |
| 8 | 110 |
| 4 | 101 |
| 2 | 100 |
| 1 | 001 |

Table 16 Conversion table between dezH and DEZHM/DEZMS

The horizontal compression/expansion block can be switched off by setting DEZHM/DEZHS equal "0" and INT HM/INT HS=2048. In this case it is possible to switch on a low pass filter for the chrominance data path by the I²C Bus parameter CHFILM/CHFILS (I²C Bus parameter, 03h,25h). If CHFILM/CHFILS is equal to "0" or "1" the horizontal filter for the chrominance is switched off. If CHFILM/CHFILS is equal to "2" or "3" the horizontal filter for the chrominance is switched on. The table below shows the different settings of CHFILM/S.

System description

| CHFILM/CHFILMS | Vertical low pass filter (only valid for DEZVM/DEZVS=0) | Horizontal low pass filter (only valid for DEZHM/DEZHS=0) |
|----------------|------------------------------------------------------------|--------------------------------------------------------------|
| 11 | Vertical filter on | Horizontal filter on |
| 10 | Vertical filter off | Horizontal filter on |
| 01 | Vertical filter on | Horizontal filter off |
| 00 | Vertical filter off | Horizontal filter off |

Table 17 Input write I²C Bus parameter CHFILM/CHFILS

In case of panorama mode the compression/expansion factor varies over one line. The figure below shows some examples.

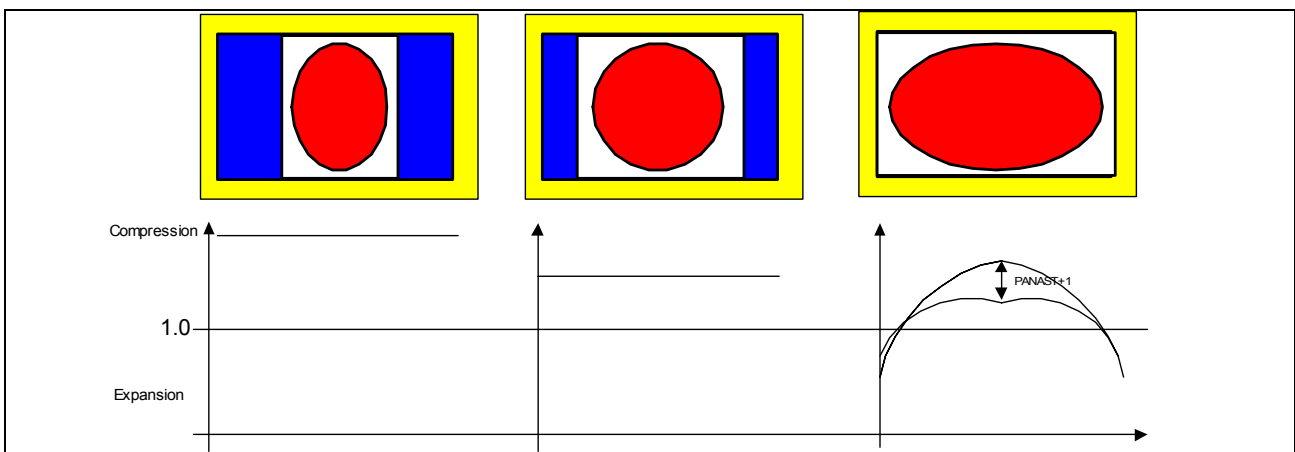


Figure 14 Principles of panorama mode

Different settings of the I²C Bus parameters INTHM/INTHS and DEZHM/DEZHS are necessary. The table below defines the settings:

| PANAON | dezH | intH |
|--------|-------------|-----------------------------|
| 0 | DEZHM/DEZHS | INTHM |
| 1 | 1 | INTHM (4096 recommended) |

Table 18 Filter I²C Bus parameter in case of PANAON=1

System description

| I ² C Bus parameter | 0 (minimum value) | 15 (maximum value) |
|--------------------------------|-------------------|--------------------|
| PANAST | slight panorama | strong panorama |

Table 19 I²C Bus parameter PANAST in case of PANAON=1

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|---------------------------------------------------------------------------------------------------------|
| INTHM | 07h,08h | Interpolation factor for horizontal compression/expansion master |
| DEZHM | 08h | Decimation factor for horizontal compression/expansion master |
| INTHS | 29h,2Ah | Interpolation factor for horizontal compression/expansion slave |
| DEZHS | 2Ah | Decimation factor for horizontal compression/expansion slave |
| APPLM | 0Eh | Number of active pixels per line in the input data stream after horizontal compression/expansion master |
| APPLS | 30h | Number of active pixels per line in the input data stream after horizontal compression/expansion slave |
| PANAON | 1Ah | Horizontal panorama mode on/off |
| PANAST | 1Ah | Gradient of horizontal panorama mode |

Table 20 Input write I²C Bus parameter

System description

5.4.3 Noise reduction

The figure below shows a block diagram of the spatial and temporal motion adaptive noise reduction (first order IIR filter). The spatial noise reduction is only performed on the luminance signal. The structure of the temporal motion adaptive noise reduction is the same for the luminance as for the chrominance signal.

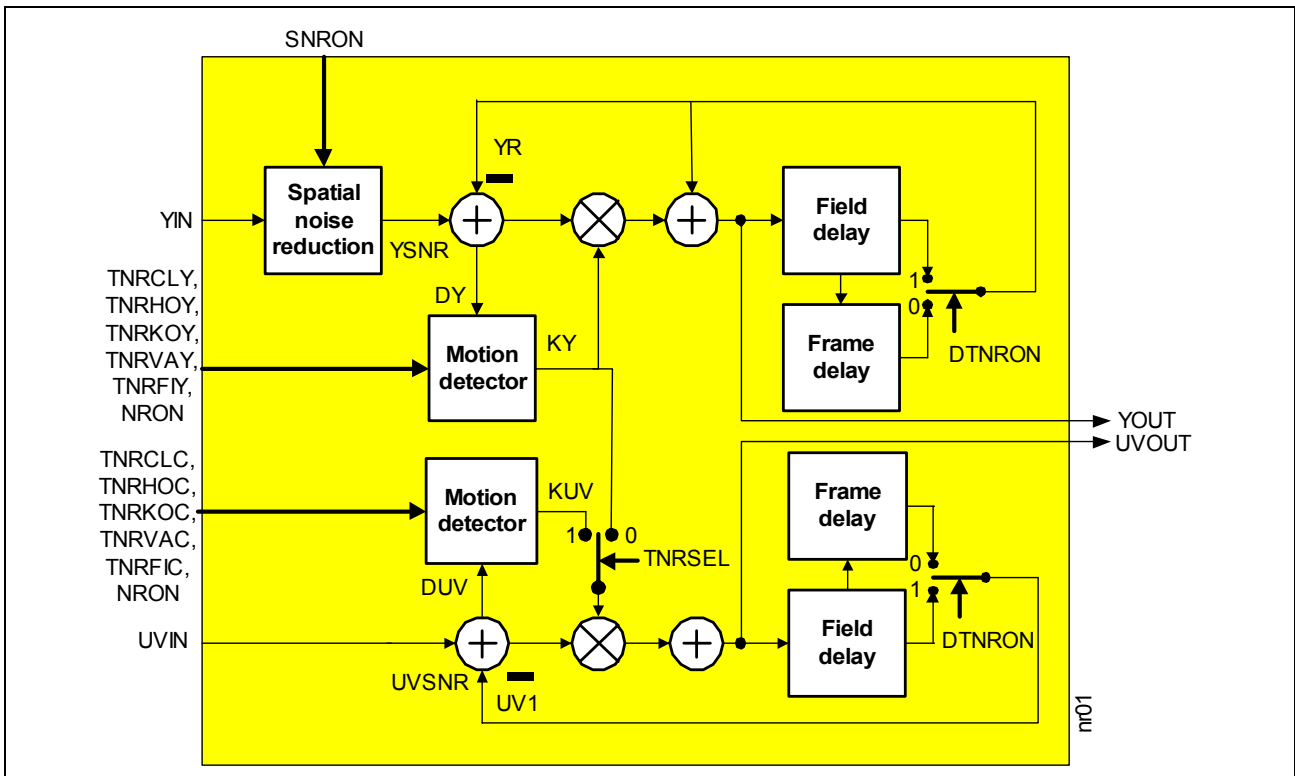


Figure 15 Block diagram of noise reduction

5.4.3.1 Spatial noise reduction

Normally a spatial noise reduction reduces the resolution due to the low pass characteristic of the used filter. Therefore the spatial noise reduction of the SDA 9415 works adaptive on the picture content. The low pas filter process is only executed on a homogeneous area.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|---------------------------------------------|
| SNRON 1: on 0: off | 1Ah | Spatial noise reduction of luminance signal |

Table 21 Input write I²C Bus parameter

System description

5.4.3.2 Motion adaptive temporal noise reduction

The equation below describes the behaviour of the temporal motion adaptive noise reduction filter. The same equation is valid for the chrominance signal. Depending on the motion in the input signal, the K-factor K_y (K_{uv}) can be adjusted between 0 (no motion) and 15 (motion) by the motion detector. The K-factor for the chrominance filter can be either K_y (output of the luminance motion detector, $TNRSEL=0$) or K_{uv} (output of the chrominance motion detector, $TNRSEL=1$). For the luminance and chrominance signal the delay of the feed back path can be either a field delay ($DTNRON=1$) or a frame delay ($DTNRON=0$) (block diagram of noise reduction).

Equation for temporal noise reduction (luminance signal)

$$Y_{OUT} = \left(\frac{1 + K_y}{16} \right) (Y_{SNR} - Y_R) + Y_R$$

Equation for temporal noise reduction (chrominance signal)

$$UV_{OUT} = \left(\frac{1 + K}{16} \right) (UV_{SNR} - UV_1) + UV_1; K = (K_y; K_{uv})$$

(compare "Block diagram of noise reduction" on page 44)

The **Figure 16** shows the motion detector in more detail. Temporal noise reduction can be switched off by $NRON$ ($NRON=0$). The I²C Bus parameter $TNRFIY/C$ switches between a fixed noise reduction K-factor $TNRVAY/C$ ($TNRFIY/C=0$) or a motion adaptive noise reduction K-factor ($TNRFIY/C=1$).

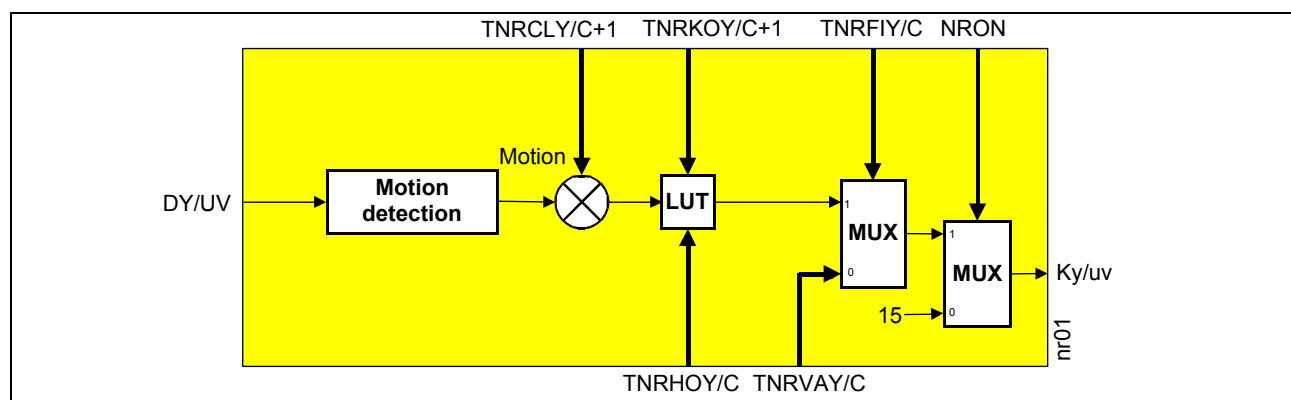


Figure 16 Block diagram of motion detector

In case of adaptive noise reduction the K-factor depends on the detected "Motion" (see **Figure 16**). The "Motion"- K_y/K_{uv} characteristic curve (LUT) is fixed inside the SDA 9415, but the characteristic curve can be changed by two I²C Bus parameters: $TNRHOY/C$ and $TNRKOY/C$. $TNRHOY/C$ shifts the curve horizontally and $TNRKOY/C$ shifts the

System description

curve vertically. For a fixed characteristic curve, the sensitivity of the motion detector is adjustable by TNRCLY/C.

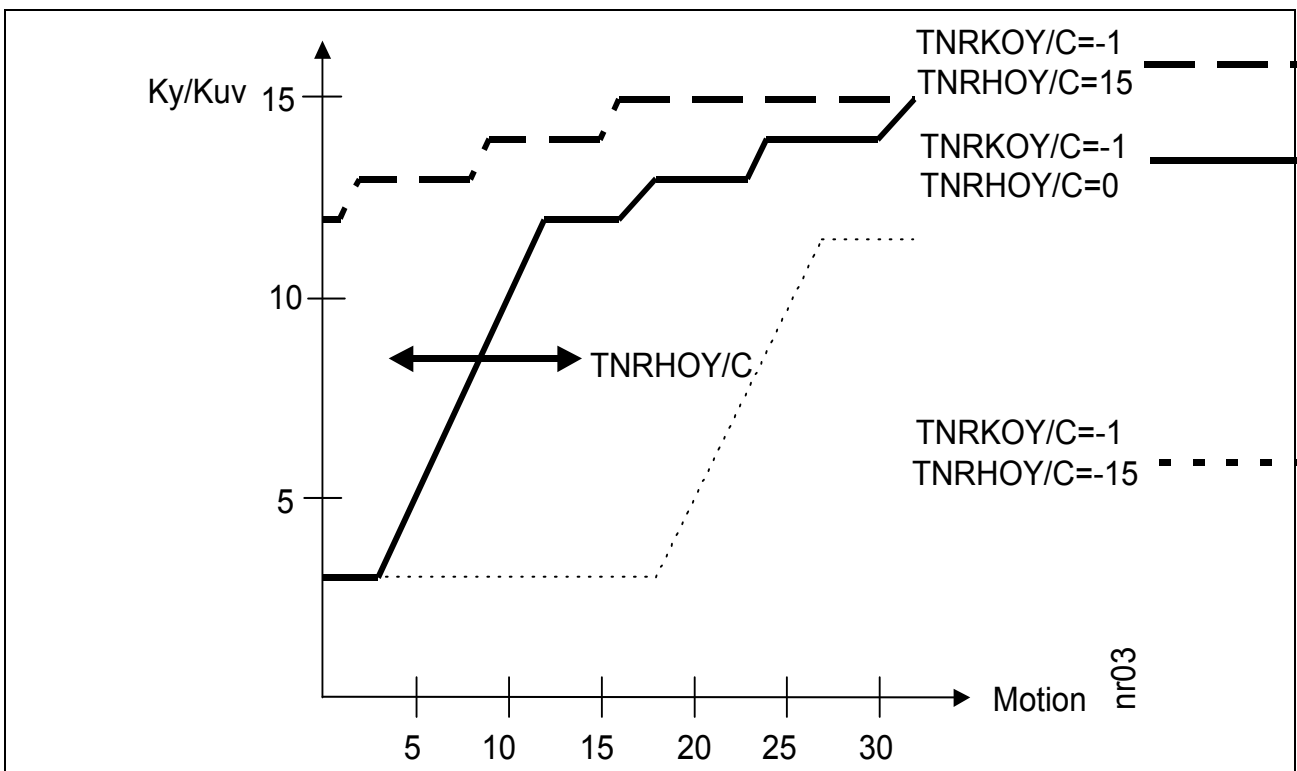
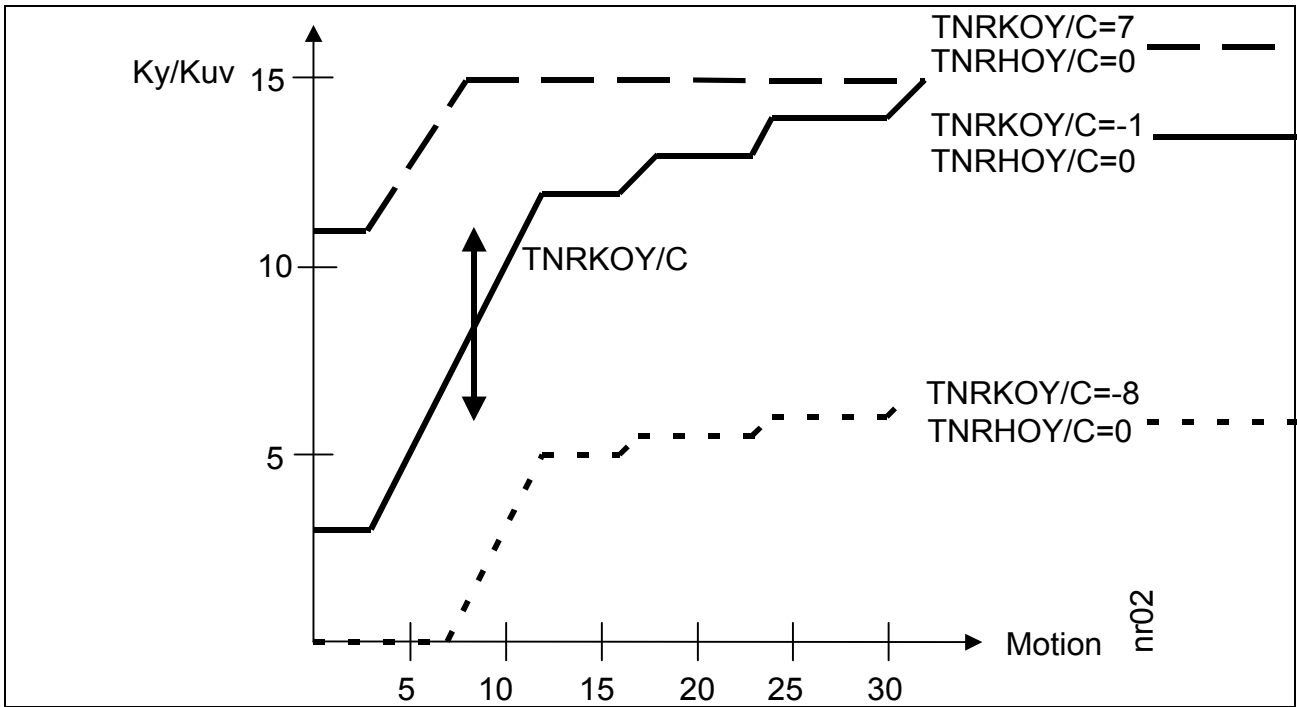


Figure 17 LUT for motion detection

System description

| I ² C Bus parameter | 0 (minimum value) | 15 (maximum value) |
|--------------------------------|-----------------------------------------------------------|--------------------------------------------------------|
| TNRVAY/C | strong noise reduction (not motion adaptive, Ky/Kuv=0) | no noise reduction (not motion adaptive, Ky/Kuv=15) |

Table 22 I²C Bus parameter TNRVAY/C

| I ² C Bus parameter | Range |
|--------------------------------|---------------|
| TNRHOY/C | -32, ... , 31 |
| TNRKOY/C | -8, ..., 7 |

Table 23 I²C Bus parameter TNRHOY/C and TNRKOY/C

| I ² C Bus parameter | 0 (minimum value) | 15 (maximum value) |
|--------------------------------|-------------------------------------------------------------|-----------------------------------------------------------|
| TNRCLY/C | maximum sensitivity for motion -> strong noise reduction | minimum sensitivity for motion -> weak noise reduction |

Table 24 I²C Bus parameter TNRCLY

System description

| I ² C Bus parameter | Sub address | Description |
|----------------------------------------------------------|-------------|-------------------------------------------------------------------------------|
| NRON 1: on 0: off | 1Ah | Temporal Noise Reduction of Luminance and Chrominance On (SRC-Mode) |
| TNRSEL 1: separate 0: luminance motion detector | 18h | Switch for motion detection of temporal noise reduction of chrominance signal |
| DTNRON 1: field 0: frame | 1Ah | Delay for temporal noise reduction of luminance and chrominance signal |
| TNRFIY/C 1: off 0: on | 18h/19h | Switch for fixed K-factor value defined by TNRVAY/C |
| TNRVAY/C | 17h | Fixed K-factor for temporal noise reduction of luminance/chrominance |
| TNRHOY/C | 18h/19h | Horizontal shift of the motion detector characteristic |
| TNRKOY/C | 16h | Vertical shift of the motion detector characteristic |
| TNRCLY/C | 15h | Classification of temporal noise reduction |

Table 25 Input write I²C Bus parameter

5.4.4 Noise measurement

The noise measurement algorithm can be used to change the I²C Bus parameters of the temporal noise reduction processing depending on the actual noise level of the input signal. This is done by the I²C Bus controller which reads the NOISEME value, and sends depending on this value different I²C Bus parameter sets to the temporal noise reduction registers of the SDA 9415. The NOISEME value can be interpreted as a linear curve from no noise (0) to strong noise (30). Value 31 indicates an overflow status and can be handled in different ways: strong noise or measurement failed.

Two measurement algorithms are included, which can be chosen by the I²C Bus parameter NMALG. In case NMALG=1 the noise is measured during the vertical blanking period in the line defined by NMLINE. For NMALG=0 the noise is measured during the first active line. In the latter case the delay of the noise reduction algorithm must be set to the frame difference value (DTNRON=0, I²C Bus sub address 1Ah). In both cases the value is determined by averaging over several fields.

The **Figure 18** shows an example for the noise measurement. The NMLINE I²C Bus parameter determines the line, which is used in the SDA 9415 for the measurement. In case of VINDEL=0 and NMLINE=0 line 3 of the field A and line 316 of the field B is

System description

chosen. In case of VINDEL=0 and NMLINE=3 line 6 of the field A and line 319 of the field B is chosen.

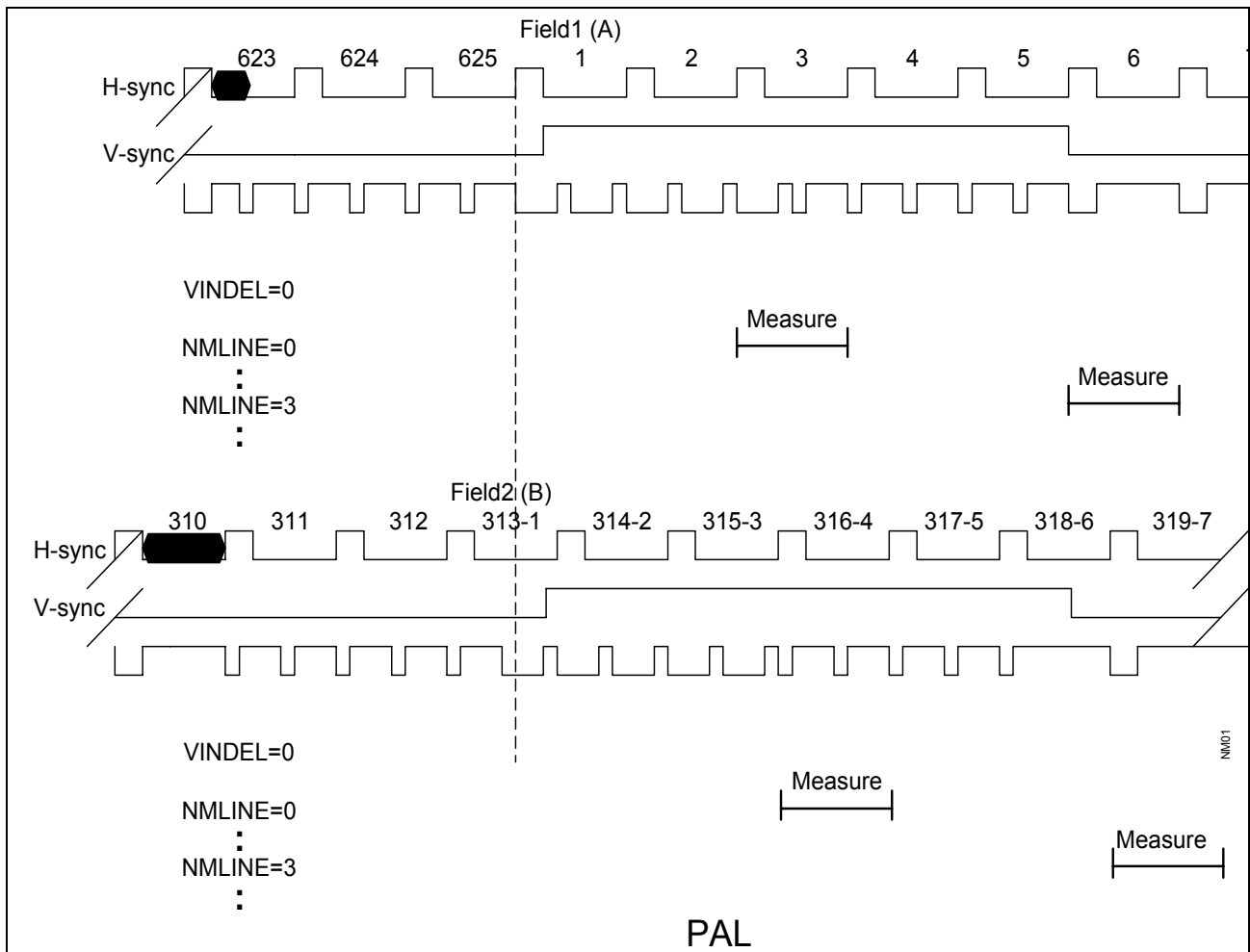


Figure 18 Example of noise measurement

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NMALG | 14h | Noise measurement algorithm 1: measurement during vertical blanking period (measure line can be defined by NMLINE) 0: measurement in the first active line |
| NMLINE | 14h | Line for noise measurement (only valid for NMALG=1) |

Table 26 Input write I²C Bus parameter

System description

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NOISEME | 7Ah | Noise level of the input signal: 0 (no noise), ... , 30 (strong noise) [31 (strong noise or measurement failed)] |
| NMSTATUS | 7Ch | Signals a new value for NOISEME 1: a new value can be read 0: current noise measurement has not been updated ("I ² C Bus" on page 123) |

Table 27 Input read I²C Bus parameter

5.4.5 Letter box detection

The **Figure 19** shows the display of a 4:3 letter box source on 16:9 tube. Black bars on the top and bottom as well as on the right and on the left are visible. It is possible by vertical and horizontal expansion to display the picture on the whole tube. Therefore only the first line (Start Line of Active Area - SLAA) and the last line (End Line of Active Area - ELAA) of the active area must be known. The letter box detection algorithm detects SLAA and ELAA. Both I²C Bus parameters can be read out via I²C Bus. The μ C of the TV chassis can use both values to calculate the corresponding zoom factor for the vertical expansion.

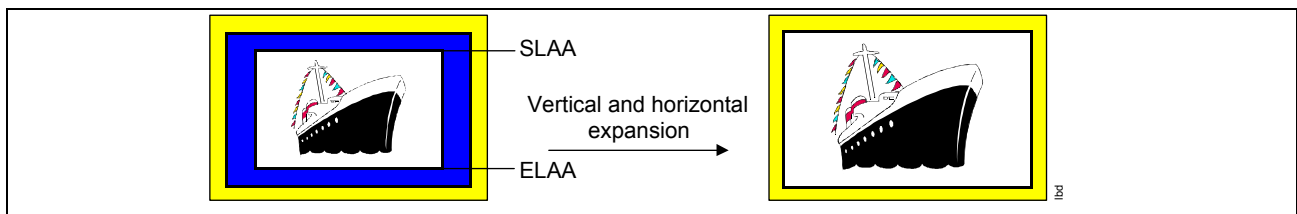


Figure 19 Principle of letter box detection

The **Figure 20** shows the block diagram of the letter box detection. The letter box algorithm processes only the luminance data. Each incoming field is processed. The default value of SLAA is NALPFIPM+PD and of ELAA is 2*ALPFIPM+NALPFIPM+PD-1 (PD - Processing Delay), which means no letter box format source material.

System description

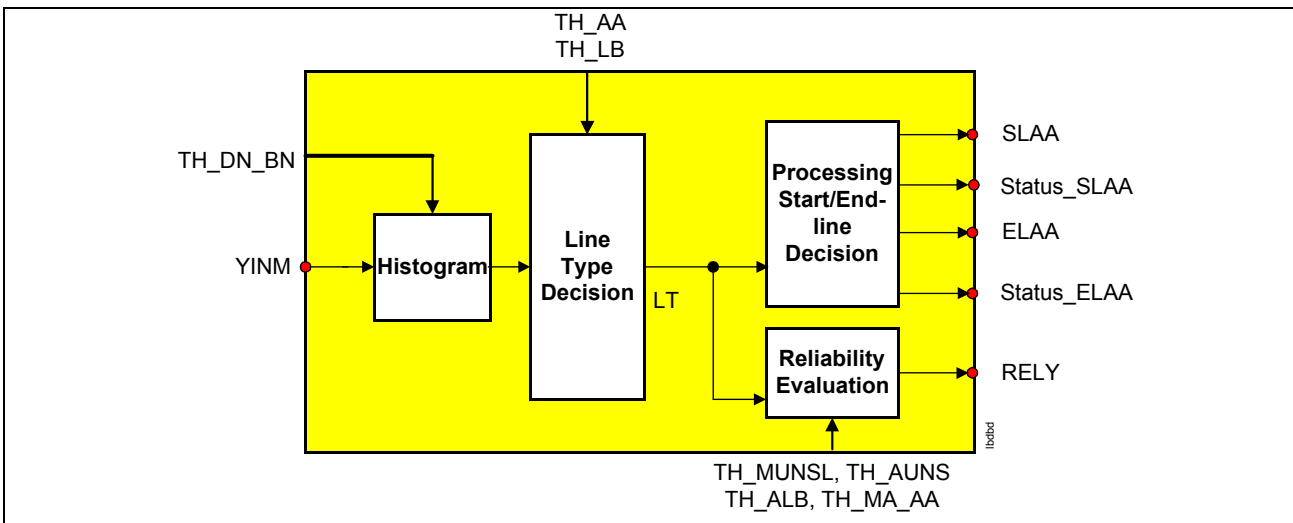


Figure 20 Block diagram of letter box detection

Each line of the input picture will be assigned to one of three line types (LT) by the “Histogram” and “Line Type decision” block. The figure below shows in detail the functionality of both blocks. The “Histogram” block counts the amount of pixels (BC), which are larger or equal $2 * TH_DN_BN$ (I²C Bus parameter, 1Ch). Depending on the counter value the line is assigned to one of the three line types by the “Line Type Decision” block. The I²C parameter TH_AA and TH_LB can be used to influence the result of the “Line Type Decision” block.

| Line Type (LT) | Priority | BC |
|----------------|----------|--------------------------------------|
| AA | 1 | $\geq 4 * TH_AA$ |
| LB | 2 | $< 4 * TH_LB$ |
| UNS | 3 | $< 4 * TH_AA$ and $\geq 4 * TH_LB$ |

Table 28 Line Type Decision of LBD

The line type AA marks lines which belong to an active area, the line type LB marks lines which belong to a letter box area (maybe including logos, subtitles) and the line type UNS marks lines which could not assigned with security to one of both line types mentioned before.

System description

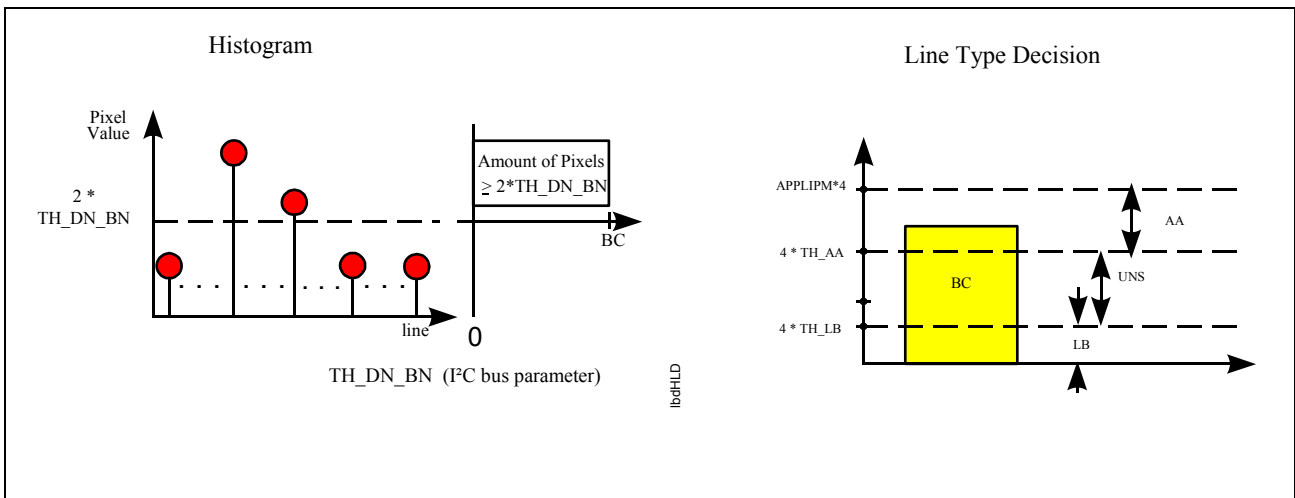


Figure 21 Histogram and line type decision

Based on the line types the first line of the active area (SLAA, I²C parameter 78h) and the last line of the active area (ELAA, I²C parameter 79h) is determined. Furthermore the information about reliability of the SLAA and ELAA value is determined. The reliability information is readable by I²C Bus of the parameters STATUS_SLAA and STATUS_ELAA. If STATUS_SLAA/STATUS_ELAA is equal “1” the SLAA/ELAA value is reliable, otherwise the SLAA/ELAA value is not reliable.

In addition a global reliability signal RELY exists, which is also readable by I²C Bus. The results of the letter box detection are reliable, if the RELY signal is read as “1”. The “Reliability evaluation” block determines the RELY signal, which can be influenced by the I²C Bus parameter TH_MUNSL, TH_AUNS and TH_ALB. The table below explains the generation of the RELY signal. The thresholds TH_MUNSL, TH_AUNS and TH_ALB are compared with internal counter values UNSLENGTH, UNSAMOUNT and LBAMOUNT, respectively. If one of the three conditions is true, the RELY signal is set to not reliable. UNSLENGTH contains the maximum length of consecutive lines with the line type UNS. UNSAMOUNT contains the amount of lines with the line type UNS and LBAMOUNT contains the amount of lines with the line type LB.

| RELY | |
|------------------|---------------------------------------------------------------------------------|
| 0 (not reliable) | UNSLENGTH > 16 * TH_MUNSL or UNSAMOUNT > 16 * TH_AUNS or LBAMOUNT > 16 * TH_ALB |
| 1 (reliable) | otherwise |

Table 29 Evaluation of the reliability signal RELY

The I²C Bus parameter TH_MA_AA can be used to force the SLAA and ELAA value to their default values. Therefore the amount of active area line types AA is counted in the

System description

upper half of the input picture (AAFH) and the lower half of the input picture (AASH). If one of both counter values is greater as $2 * TH_MA_AA + 112$, the SLAA and ELAA I²C Bus parameters are set to their default values.

| Output signals | |
|----------------------------------------------------------------------------------|--------------------------------------------|
| SLAA=NALPIPM+PD ELAA=2*ALPFIPM+SLAA-1 Status_SLAA=TRUE Status_ELAA=TRUE | (AAFH or AASH) $\geq 2 * TH_MA_AA + 112$ |
| no change of the values | otherwise |

Table 30 Correction of “start/end-line decision filter” block

It is possible to make the results of the letter box detection visible on screen in real time to optimize the I²C Bus parameters. The figure below explains the different possibilities. The I²C Bus parameter VOLBD can be used to switch on (VOLBD=1) or off (VOLBD=0) the visibility function.

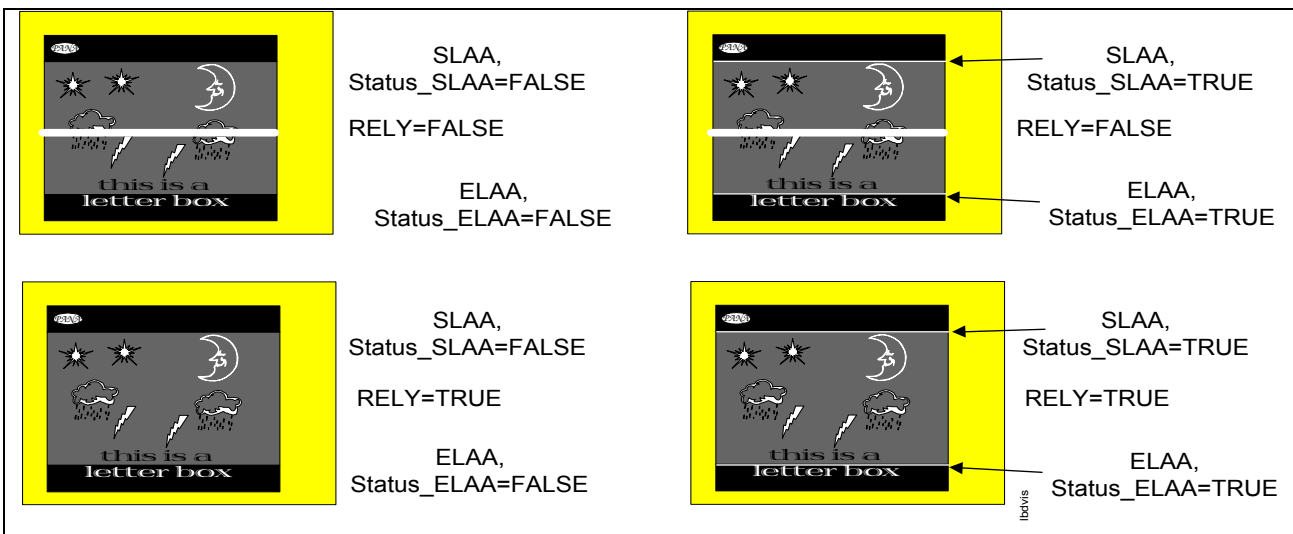


Figure 22 Visibility of letter box detection I²C Bus parameters

System description

| I ² C Bus parameter [default] | Sub address | Description |
|------------------------------------------|-------------|---------------------------------------------------------------------------|
| TH_DN_BN [15] | 1Ch | Darkness Brightness threshold |
| TH_LB [12] | 1Ch,1Dh | Letter box threshold |
| TH_ALB [6] | 1Dh | Amount of letter box threshold |
| TH_AA [50] | 1Eh | Active area threshold |
| TH_MUNSL [5] | 1Fh | Maximum length of insecure threshold |
| TH_AUNS [7] | 1Fh | Amount of letter box and insecure threshold |
| TH_MA_AA [14] | 20h | Maximum amount of active area threshold |
| VOLBD [0] | 20h | Makes result of letter box detection visible on screen 1: on 0: off |

Table 31 Input write I²C Bus parameter

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SLAA | 78h | First line of active area = 2 * SLAA |
| ELAA | 79h | Last line of active area = 2 * ELAA |
| STATUS_SLAA | 7Bh | Status of SLAA 1: SLAA is reliable 0: SLAA is not reliable |
| STATUS_ELAA | 7Bh | Status of ELAA 1: ELAA is reliable 0: ELAA is not reliable |
| RELY | 7Bh | Reliability signal: 1: All values of letter box detection are reliable 0: All values of letter box detection are not reliable |
| LBDSTATUS | 7Ch | Signals new values for letter box detection 1: new values can be read 0: current letter box detection measurement not finalized ("I ² C Bus" on page 123) |

Table 32 Input read I²C Bus parameter

System description

5.5 Clock concept

| Signals | Pin number | Description |
|---------|------------|------------------------------------|
| CLKM | 18 | System clock input master channel |
| CLKS | 58 | System clock input slave channel |
| X1/CLKD | 2 | System clock input display channel |

Table 33 Input signals

| Signals | Pin number | Description |
|---------|------------|--------------|
| CLKOUT | 3 | Clock output |

Table 34 Output signals

The SDA 9415 supports different clock concepts. The **Figure 24** shows a typical application of the SDA 9415. The frontend clock is connected to CLKM input. The second frontend clock is connected to CLKS input. The CLKOUT pin is connected to the backend and the X1/CLKD input is connected to a crystal oscillator. The **Figure 23** explains the clock switch, which may be used for the separate modes (see also **Table 37 "Ingenious configurations of the HOUT and VOUT generator" on page 84**).

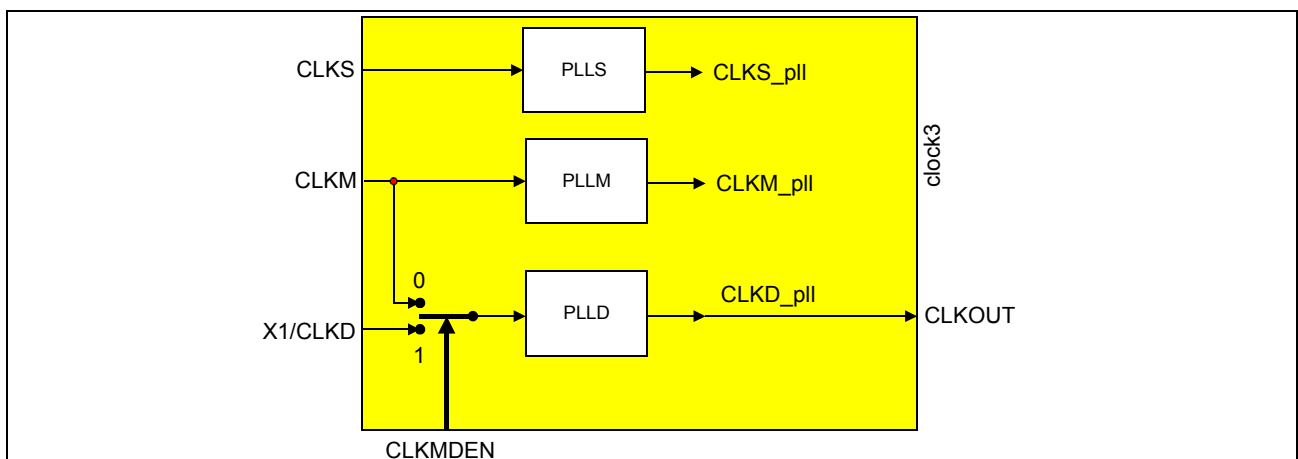


Figure 23 Clock concept of SDA 9415

System description

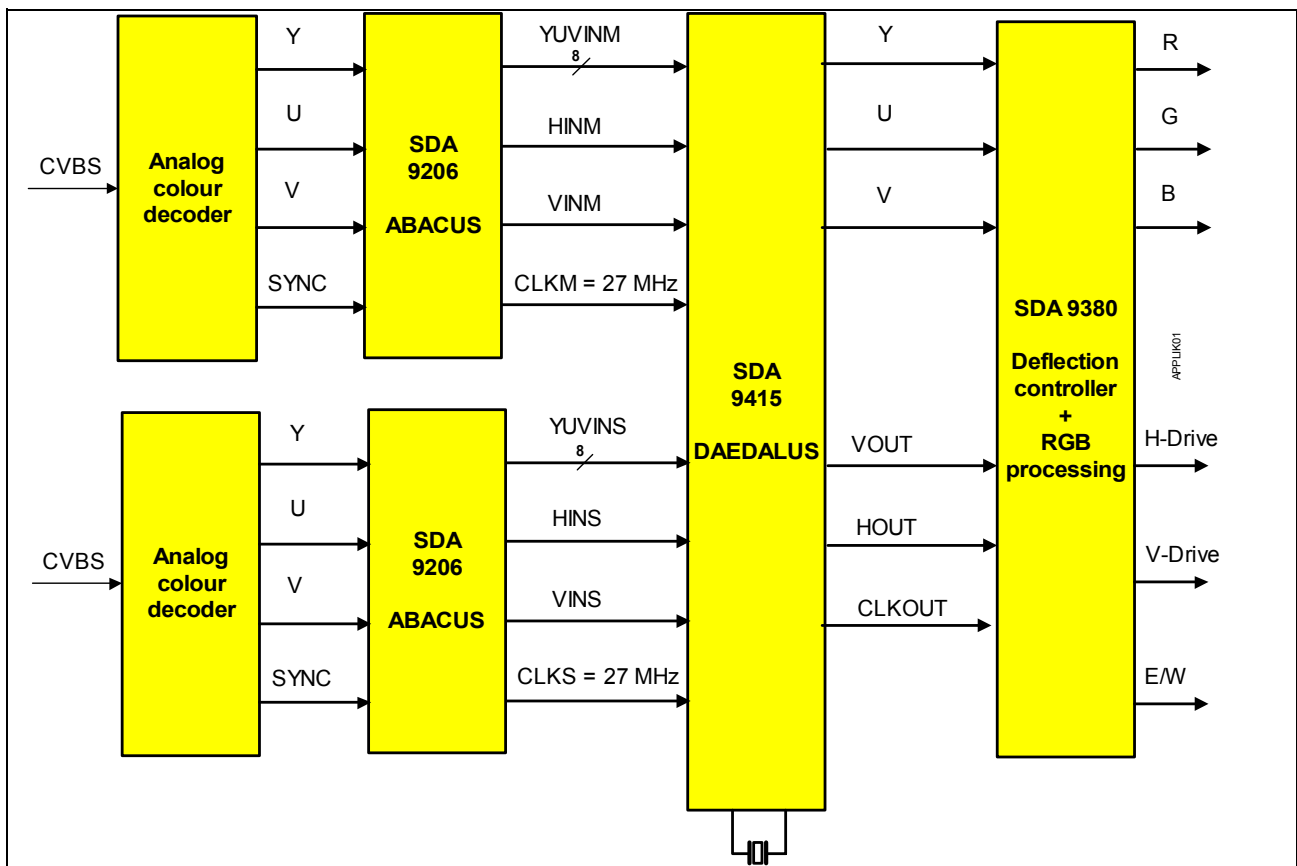


Figure 24 Application for SDA 9415

| CLKMDEN (5Fh) | PLL input |
|---------------|-----------|
| 0 | CLKM |
| 1 | X1/CLKD |

| Clock | Used in block |
|----------|--------------------------------------------------------------------------------|
| CLKM_pll | ISCM, IFCM, VHCOMM, TSNR, LBD, LM, I ² C |
| CLKS_pll | ISCS, IFCS, VHCOMS, LM, I ² C |
| CLKD_pll | OSCM/S, ME, SRCM, SRCS, ED, MC, LM, DLTi, DCTi, Peaking, DAC, I ² C |

Table 35 Clock concept switching matrix

System description

| I ² C Bus parameter | Sub address | Description |
|---------------------------------------|-------------|--------------------------------------------------------------|
| PLLMOFF 1: off 0: on | 00h | PLLM master channel on or off, only for test purpose |
| PLLMRA | 00h | PLLM range, only for test purpose |
| PLLSOFF 1: off 0: on | 22h | PLLS slave channel on or off, only for test purpose |
| PLLSRA | 22h | PLLS range |
| PLLD OFF 1: off 0: on | 5Fh | PLLD display channel on or off, only for test purpose |
| PLLDRA | 5Fh | PLLD range |
| CLKOUTON 1: enabled 0: disabled | 5Fh | Output of system clock CLKOUT |
| CLKMDEN 1: X1/CLKD 0: CLKM | 5Fh | Input clock for PLLD |

Table 36 Input write I²C Bus parameter

5.6 Application modes and memory concept

5.6.1 Introduction

The Main Memory of the SDA 9415 has an overall capacity of 6 Mbit. It is divided into two identical and independent 3 Mbit parts.

The Main Memory has 2 completely independent data inputs (master and slave channel) to enable a multitude of PIP features. In general the channels are asynchronous having 2 separate clock PLLs (CLKM, CLKS). Reading of master and slave data for display is performed using a third asynchronous clock (CLKD). In this way a decoupling of input and output clocks is achieved.

The Main Memory supports different operation modes of the SDA 9415 by adapted data configurations. The different modes are defined by the I²C Bus parameter MEMOP (I²C Bus sub address 53h).

System description

| MEMOP | Memory operation mode |
|-------|-----------------------------------|
| 00 | SRC-Mode (Sample Rate Conversion) |
| 01 | SSC-Mode (Split screen) |
| 10 | MUP-Mode (Multi picture) |
| 11 | not defined |

Table 37 Definition of MEMOP

In SRC operation mode the capacity to store 2 fields of the luminance and chrominance components of the master channel is supplied (4:1:1 or 4:2:0 format, I²C Bus parameter CHRFORM/CHRFORS, 12h/34h).

| CHRFORM | Data format |
|---------|-------------|
| 00 | 4:1:1 |
| 01 | 4:2:0 |
| 1X | reserved |

| CHRFORS | Data format |
|---------|-------------|
| 0 | 4:1:1 |
| 1 | 4:2:0 |

Table 38 Definition of CHRFORM/CHRFORS

The **Figure 25** shows the differences between the 4:1:1, 4:2:2 and 4:2:0 data format.

System description

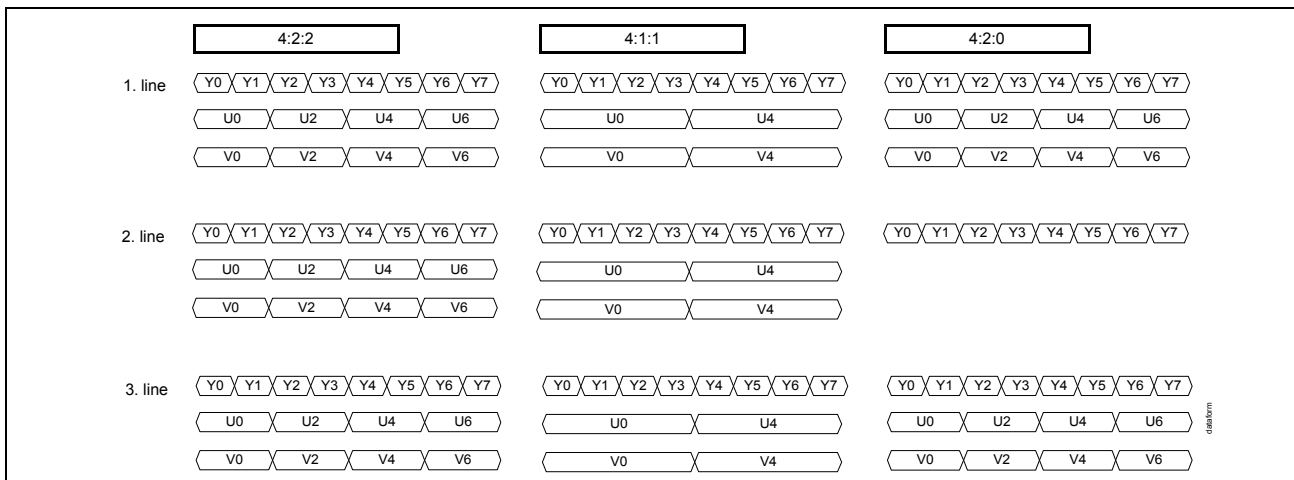


Figure 25 Supported data formats

Additionally 3 fields of a decimated picture of the slave channel with the size of up to 1/9 of the original format can be stored (4:1:1 or 4:2:0 format). In this mode motion estimation and compensation (Micronas VDU algorithm) for the master channel is supported (up to 30 MHz clock frequency). In parallel it is possible to insert the slave channel at any display position using frame mode and without joint lines. Noise reduction algorithm by recursive filtering is supported only for the master channel in SRC-Mode.

In SSC-Mode the data configuration of master and slave channel can be different. Depending on the picture size it is possible to store only 1 field of luminance and chrominance data or 2 fields. The data configuration can be defined by the I²C Bus parameters ORGMEMM and ORGMEMS, respectively.

| ORGMEMM | Data configuration of the memory |
|---------|------------------------------------------------------|
| 1 | 2 fields (limited picture size in SSC- and MUP-Mode) |
| 0 | 1 field |

Table 39 Definition of ORGMEMM

| ORGMEMS | Data configuration of the memory |
|---------|-------------------------------------------------------------------------------------------------------|
| 1 | 3 fields PIP (SRC-Mode), 2 fields (restricted picture size, SSC and MUP Mode) |
| 0 | Slave channel blocked (SRC-Mode and ORGMEMM=1) 1 field (SSC- and MUP-Mode; SRC-Mode and ORGMEMM=0) |

Table 40 Definition of ORGMEMS

System description

Having 2 fields available for the master channel joint line free display can be activated. Storing 2 fields for both channels a complete joint line free display is possible. In both cases a suitable shift of the output raster phase is necessary (especially for 'Double Window' / 'Split Screen' / 'Picture And Picture' / 'Side by Side'). In SSC mode field repetition (Simple 100Hz AABB; Field repetition AAAA or BBBB) is used for interlaced scan (100/120 Hz) rate conversion, ABAB modes are not supported. For progressive scan conversion also only field based algorithms are possible (Simple 50Hz AA*, B*B; Field repetition AA*, B*B). For the definition of the different scan rate conversion algorithms compare "**Operation mode generator**" on page 87.

Positioning of the pictures on the display is done externally by specifying the start of reading for both channels.

In MUP-Mode the configurations and functions for both channels are programmable independently. Two fields of the master channel can be stored to achieve a joint line free display of one decimated live picture. Applying smaller decimation factors only one field can be stored and joint line free display is not possible any more. These 2 modes correspond to SSC configuration for the master channel, AABB mode is supported.

For the second channel or for both channels any number of decimated fields can be stored step by step. The horizontal positions of the pictures are adjustable in steps of 4 pixel, the vertical positions are also variable and have a step size of 2 lines. The width and the height of a decimated picture depend on the corresponding decimation factors. A maximum of 1 picture per channel can be live. Only field repetition (AAAA, BBBB) is supported in this mode. Other display modes cause raster artefacts in live pictures. Joint lines are also not removed in live pictures.

A special MUP-Mode based on SSC memory configuration enables storing of 2 fields of a decimated still picture. The fields are calculated using only one input field for decimation. The generated lines are interpreted alternating as A- and B-lines. The described method improves vertical resolution of still pictures clearly without causing motion artefacts. The limited memory capacity does not allow to fill the complete display with decimated pictures created with the described method using only one channel. The different configuration can be selected by the I²C Bus parameter VERRESM and VERRESS, respectively.

| VERRESM/VERRESS | Vertical resolution in MUP-Mode (ORGMEMM/ORGMEMS=1 and WRFLDM/WRFLDS=1) |
|-----------------|----------------------------------------------------------------------------|
| 1 | frame resolution |
| 0 | field resolution |

Table 41 **Definition of VERRESM/VERRESS**

System description
5.6.2 Configuration controlling

The following **Table 42** and **Table 43** summarize all possible combinations of memory data configurations for the master and slave channel and the corresponding applications. The main configurations are no. 1 for motion compensated up conversion and PIP insertion, no. 5 for joint line free Split Screen display and no. 9 for high quality Multi Picture including one live channel.

Table 44 shows the possible picture sizes. The data formats can be always 4:2:0 or 4:1:1. In SSC and MUP mode the picture sizes are influenced by the I²C Bus parameters MEMWRM and MEMWRS.

| Config. | MEMOP | ORGMEMM | ORGMEMS | Master Channel | | Slave Channel | |
|---------|-------|---------|---------|----------------|---|---------------|--------|
| | | | | Fields | | Fields | |
| | | | | Y | C | Y | C |
| 1 | 00 | 1 | 1 | 2 | 2 | 3 | 3 |
| 2 | 00 | 1 | 0 | 2 | 2 | not available | |
| 3 | 00 | 0 | 1 | 1 | 1 | 3 2 | 3 2 |
| 4 | 00 | 0 | 0 | 1 | 1 | 1 | 1 |
| 5 | 01 | 1 | 1 | 2 | 2 | 2 | 2 |
| 6 | 01 | 1 | 0 | 2 | 2 | 1 | 1 |
| 7 | 01 | 0 | 1 | 1 | 1 | 2 | 2 |
| 8 | 01 | 0 | 0 | 1 | 1 | 1 | 1 |
| 9 | 10 | 1 | 1 | 2 | 2 | 2 | 2 |
| 10 | 10 | 1 | 0 | 2 | 2 | 1 | 1 |
| 11 | 10 | 0 | 1 | 1 | 1 | 2 | 2 |
| 12 | 10 | 0 | 0 | 1 | 1 | 1 | 1 |

Table 42 Programmable data configurations

System description

| Config. | Mode | Application |
|---------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | SRC | motion compensated up conversion (4:1:1 or 4:2:0) + PIP (ABAB, frame based) |
| 2 | SRC | motion compensated up conversion with enlarged picture size, no PIP facility |
| 3 | SRC | AABB conversion for master and slave channel, slave data is written twice (PIP- and SSC-configuration) used during switching from configuration 1 to configuration 7 without artefacts |
| 4 | SRC | 2 independent not synchronized full size channels, AABB conversion |
| 5 | SSC | joint line free 'Double Window' / 'Split Screen' / 'PAP' display, AABB conversion |
| 6 | SSC | display of 2 live channels, AABB conversion slave channel exceeds the maximum double window size |
| 7 | SSC | display of 2 live channels, AABB conversion master channel exceeds the maximum double window size |
| 8 | SSC | 2 independent not synchronized full size channels, AABB conversion |
| 9 | MUP | high resolution Multi Picture for master and slave channel (one live picture possible) AABB conversion |
| 10 | MUP | high resolution Multi Picture for master channel, reduced resolution Multi Picture for slave channel, AABB conversion |
| 11 | MUP | reduced resolution Multi Picture for master channel, high resolution Multi Picture for slave channel, AABB conversion |
| 12 | MUP | reduced resolution Multi Picture for master and slave channel, AABB conversion |

Table 43 Applications of different data configurations

System description

| Config. | Master Channel | | Slave Channel | |
|---------|----------------------|-----------|-----------------------|-----------|
| | Size [Pixel X Lines] | | Size [Pixel X Lines] | |
| | MEMWRM=0 | MEMWRM=1 | MEMWRS=0 | MEMWRS=1 |
| 1 | 768 X 288 | | 256 X 104 | |
| 2 | 768 X 341 | | not available | |
| 3 | 768 X 288 | | 256 X 104 / 512 X 176 | |
| 4 | 768 X 341 | | 768 X 341 | |
| 5 | 512 X 256 | 768 X 170 | 512 X 256 | 768 X 170 |
| 6 | 512 X 256 | 768 X 170 | 512 X 512 | 768 X 341 |
| 7 | 512 X 512 | 768 X 341 | 512 X 256 | 768 X 170 |
| 8 | 512 X 512 | 768 X 341 | 512 X 512 | 768 X 341 |
| 9 | 512 X 256 | 768 X 170 | 512 X 256 | 768 X 170 |
| 10 | 512 X 256 | 768 X 170 | 512 X 512 | 768 X 341 |
| 11 | 512 X 512 | 768 X 341 | 512 X 256 | 768 X 170 |
| 12 | 512 X 512 | 768 X 341 | 512 X 512 | 768 X 341 |

Table 44 Maximum picture sizes

| MEMWRS | Memory write mode slave channel |
|--------|---------------------------------|
| 1 | max. 768 pixel/line |
| 0 | max. 512 pixel/line |

Table 45 Definition of MEMWRS

| MEMWRM | Memory write mode master channel (ORGMEM=01 or 10, SSC or MUP Mode) |
|--------|---------------------------------------------------------------------|
| 1 | max. 768 pixel/line |
| 0 | max. 512 pixel/line |

Table 46 Definition of MEMWRM

System description

| I ² C Bus parameter [Default] | Sub address | Description |
|------------------------------------------|-------------|-------------------------------------------------|
| CHRFORM [0] | 12h | Chrominance data format master channel |
| CHRFORS [0] | 34h | Chrominance data format slave channel |
| ORGMEMM [1] | 58h | Data configuration of the memory master channel |
| ORGMEMS [1] | 57h | Data configuration of the memory slave channel |
| MEMOP [00] | 53h | Memory operation mode |
| VERRESM [0] | 58h | Vertical resolution master channel |
| VERRESS [0] | 57h | Vertical resolution slave channel |
| MEMWRM [0] | 58h | Memory write mode master channel |
| MEMWRS [0] | 57h | Memory write mode slave channel |

Table 47 Input write I²C Bus parameter

5.6.3 SRC mode configuration

Conditions: MEMOP=00, ORGMEMM=1, ORGMEMS=1

The described data configuration is typical for normal SRC mode with motion compensated 100 Hz ABAB conversion and joint line free frame based PIP insertion.

| |
|---------------------------------------------------------------|
| maximum picture size (master Channel) : 768 pixel X 288 lines |
|---------------------------------------------------------------|

| |
|--------------------------------------------------------------|
| maximum picture size (slave channel) : 256 pixel X 104 lines |
|--------------------------------------------------------------|

5.6.4 SSC and MUP mode configuration

Conditions: MEMOP=01 or 10, ORGMEMM=1, ORGMEMS=1

System description

This is the typical configuration needed for joint line free 'Split Screen' / 'Double Window' or 'PAP' display in 4:1:1 or 4:2:0 format using AABB conversion. The same configuration can be used for Multi Picture mode displaying a joint line free live picture and multiple high resolution still pictures.

maximum picture size (master and slave) : 512 (768) pixel X 256 (170) lines

In MUP-Mode it is possible to write only A fields into the memory. Therefore the I²C Bus parameters

WRFLDM and WRFLDS can be used.

| WRFLDM / WRFLDS | Write field (MUP-Mode, MEMOP=10) |
|-----------------|---------------------------------------------------------|
| 1 | only A fields are written |
| 0 | all fields are written corresponding to the actual mode |

Table 48 Definition of WRFLDM/WRFLDS

| I ² C Bus parameter [Default] | Sub address | Description |
|------------------------------------------|-------------|---------------------------------------|
| WRFLDM [0] | 58h | Write field master channel (MUP-Mode) |
| WRFLDS [0] | 57h | Write field slave channel (MUP-Mode) |

Table 49 Input write I²C Bus parameter

5.6.5 Configuration switch

This chapter deals with the switching between the different operation modes without causing visible picture artifacts. The typical application concerns the transition from SRC-PIP mode to SSC double window mode (see **figure 26 on page 67** and **figure 27 on page 68**) and furthermore to an exchange of master and slave channel (see **figure 28 on page 69**).

System description

| ORGMEMM | Data configuration of the memory (Master Channel) |
|----------------|--------------------------------------------------------------------------------------------------------------|
| 0 | SRC mode, ORGMEMM=1: no slave channel available SRC mode, ORGMEMM=0, SSC- and MUP-mode: 1 field is stored |
| 1 | SRC-mode: 3 fields are stored for PIP SSC- and MUP-mode: 2 fields are stored |

Table 50 Definition of ORGMEMM

| ORGMEMS | Data configuration of the memory (Slave Channel) |
|----------------|--------------------------------------------------------------------------------------------------------------|
| 0 | SRC mode, ORGMEMM=1: no slave channel available SRC mode, ORGMEMM=0, SSC- and MUP-mode: 1 field is stored |
| 1 | SRC-mode: 3 fields are stored for PIP SSC- and MUP-mode: 2 fields are stored |

Table 51 Definition of ORGMEMS

| MEMRDM | Memory read mode master channel (SRC-Mode, MEMOP=00) |
|---------------|-------------------------------------------------------------|
| 1 | Reading only field memory area for AABB conversion |
| 0 | Reading both field memory areas for ABAB conversion |

Table 52 Definition of MEMRDM

| MEMRDS | Memory read mode slave channel (SRC-Mode, MEMOP=00) |
|---------------|------------------------------------------------------------------|
| 1 | Reading data in PIP-configuration (joint line free, ABAB) |
| 0 | Reading data in SSC-configuration, 1 or 2 decimated fields, AABB |

Table 53 Definition of MEMRDS

System description

| MEMWRM | Memory read mode master channel (only for SSC- and MUP-mode) |
|--------|-----------------------------------------------------------------|
| 0 | 512 pixel / line |
| 1 | 768 pixel / line |

Table 54 Definition of MEMWRM

| MEMWRS | Memory read mode slave channel |
|--------|-------------------------------------------------------------------------------------------------------|
| 0 | SRC-mode: writing data in PIP configuration SSC- and MUP-mode: 512 pixel / line |
| 1 | SRC-mode: writing data in PIP- <u>and</u> in SSC configuration SSC- and MUP-mode: 768 pixel / line |

Table 55 Definition of MEMWRS

A typical animated transition to a double window display can be divided into two parts: changing the operation mode from SRC to SSC (figure 26 on page 67) and changing the picture sizes and positions continuously according to a double window display (**figure 27 on page 68**). In SSC mode no vector driven up conversion modes are possible. Only field based algorithms are supported. The corresponding I²C commands are summarized in **Table 56** and **Table 57**.

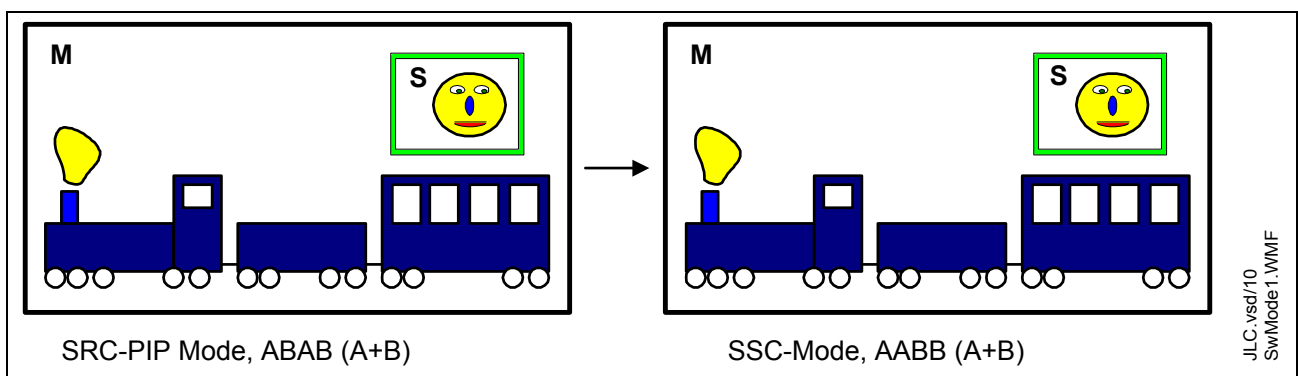


Figure 26 Switching from SRC-PIP mode to SSC mode

System description

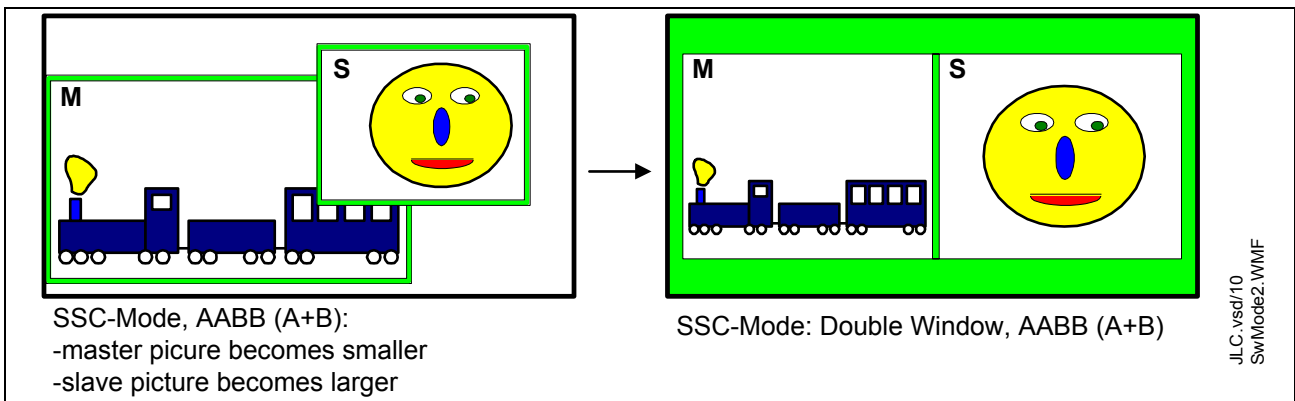


Figure 27 Changing picture sizes to get a double window display

| Steps | MEM-OP | ORG-MEMM | ORG-MEMS | MEM-WRM | MEM-WRS | MEM-RDS | MEM-RDM | Operation |
|-------|--------|----------|----------|---------|---------|---------|---------|-----------------------------------------------------------------------------------------------------------------------------------|
| 1 | 00 | 1 | 1 | 0 | 0 | 0 | 0 | SRC mode with 1/9 PIP insertion |
| 2 | 00 | 1 | 1 | 0 | 0 | 0 | 0 | a field based up conversion mode must be programmed by STOPMOM and STOPMOS |
| 2a* | 00 | 1 | 1 | 0 | 0 | 0 | 1 | only one field is read for master channel (reduced vertical resolution) |
| 3 | 00 | 0 | 1 | 0 | 1 | 0 | X | memory capacity of master channel is reduced to 1 field memory organization of slave channel is prepared for SSC configuration |
| 4 | 00 | 0 | 1 | 0 | 1 | 1 | X | slave channel reading is switched to SSC memory configuration |
| 5 | 01 | 0 | 1 | 1 | 0 | X | X | SSC mode: full size master picture, 1/9 size of slave picture |

Table 56 Switching from SRC PIP mode to SSC mode

* Step 2a may be left out

System description

| Steps | MEM-OP | ORG-MEMM | ORG-MEMS | MEM-WRM | MEM-WRS | MEM-RDS | Operation |
|-------|--------|----------|----------|---------|---------|---------|------------------------------------------------------------------------------------------------------------------------|
| 6 | 01 | 0 | 1 | 1 | 0 | X | changing picture sizes of master and slave by programming the corresponding decimation I ² C Bus parameters |
| 7 | 01 | 1 | 1 | 0 | 0 | X | reducing the width below 512 pixel for the master picture two fields can be stored |

Table 57 Changing the picture sizes to double window format

Starting in SRC mode with a PIP insertion (step 1) at first a field based up conversion mode must be chosen for both channels, e.g. AABB conversion for interlaced modes and intrafield interpolation for progressive modes (step 2). Now the capacity for the master channel can be reduced to 1 field (step 3). The free memory capacity is used to write the slave data at two address areas in parallel corresponding to SRC-PIP configuration and SSC configuration. In step 4 the reading of the slave channel data is switched to SSC configuration. In the last step also the master channel is switched to SSC mode. In this configuration we can store 1 field of the master channel and 2 fields of the slave channel. The Joint Line Controller can be activated and joint line free display is possible.

Reducing the size of the master picture and enlarging the slave picture size is performed in step 6 in table . During this phase we can get problems with joint line free display of the master picture until the horizontal width is below 512 pixel. Now also the master channel is enabled to store 2 fields and joint line free display is possible again (step 7). In this configuration double window display is performed.

During all steps positioning of both pictures is free programmable to enable multiple variations of the animation.

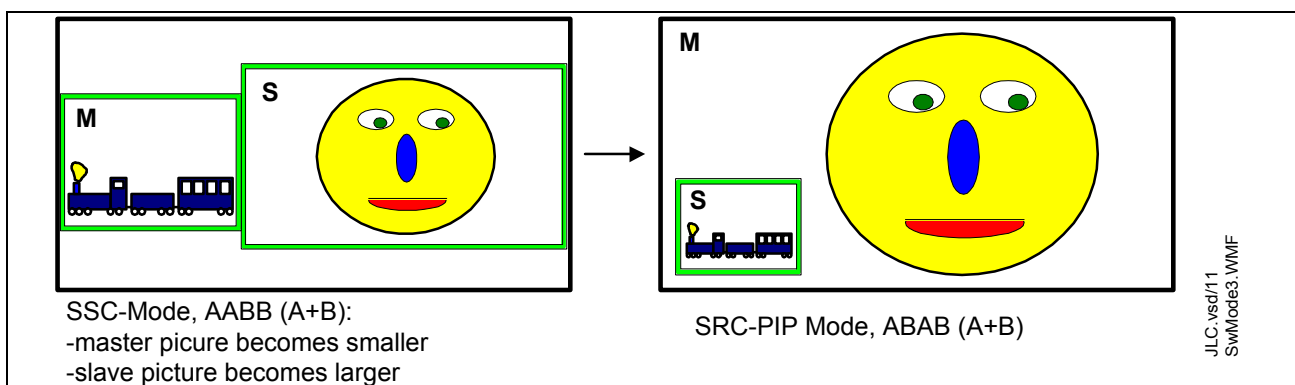


Figure 28 Completing the operations to a master slave exchange

System description

| Steps | MEM-OP | ORG-MEMM | ORG-MEMS | MEM-WRM | MEM-WRS | MEM-RDS | Operation |
|-------|--------|----------|----------|---------|---------|---------|------------------------------------------------------------------------------------------------------------------------|
| 8 | 01 | 1 | 1 | 0 | 0 | X | changing picture sizes of master and slave by programming the corresponding decimation I ² C Bus parameters |
| 9 | 01 | 1 | 0 | 0 | 1 | X | exceeding a width of 512 pixel for the slave picture only one field can be stored |
| 10 | 01 | 1 | 0 | 0 | 1 | X | further changes of picture sizes until full size slave picture and 1/9 size master picture is displayed |
| 11 | 01 | 0 | 1 | 1 | 0 | X | switching synchronization to slave channel and exchanging the inputs |
| 12 | 00 | 0 | 1 | 0 | 1 | 1 | switching to SRC mode using still field based up conversion |
| 13 | 00 | 0 | 1 | 0 | 1 | 0 | slave channel reading is switched to SRC memory configuration |
| 14 | 00 | 1 | 1 | 0 | 0 | 0 | also the master channel works frame based |
| 15 | 00 | 1 | 1 | 0 | 0 | 0 | programming STOPMOM and STOPMOS to frame based up conversion |

Table 58 Performing a master slave exchange

Starting with the double window configuration (**figure 27 on page 68**) the procedure is continued with an animation to perform an exchange of the master and slave sources to get a display like it is shown in **figure 28 on page 69**.

In step 8 the picture size of the master channel is decreased and the size of the slave picture is increased continuously. When the width of the slave picture exceeds 512 pixel only one field can be stored (step 9). Joint line free display of the slave channel is not always possible in this configuration. When full size slave picture format and 1/9 master picture size is reached (step 10) an exchange of master and slave channel is possible. Unstable picture phases can be avoided when the display raster phase is adapted to the slave channel before the hardware exchange of both sources is done. For display phase raster shifting see "**Master slave switch**" on page 72.

Now we can activate the SRC mode again. At first we just change the mode maintaining the field based conversions (step 12). Then the slave data configuration of the memory is changed to SRC configuration (step 13) and at last the master channel memory capacity is enlarged to 2 fields (step 14) and frame based up conversion modes are enabled (step 15).

System description

5.6.6 Joint line free display

This chapter describes the I²C Bus parameters to get a joint line free display in SSC mode.

| I ² C Bus parameter [Default] | Sub address | Description |
|------------------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| RSHFTM [0] | 55h | Joint line free display of master channel by shifting the output raster phase (SSC-Mode) 1: enabled 0: disabled |
| RSHFTS [0] | 55h | Joint line free display of master and slave channel by shifting the output raster phase (SSC-Mode, RSHFTM=1) 1: enabled 0: disabled |
| SHFTSTEP [0100] | 55h | Increment for raster phase shift per output frame (lines) |
| PROG_THRES [0111100] | 56h | Threshold to display progressive PIP without joint lines |

Table 59 Input write I²C Bus parameter

| I ² C Bus parameter | Description |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| SHIFACT | indicates active shifting process of the display raster phase 0: display phase shifting not active 1: display phase shift active |

Table 60 Output read I²C Bus parameter

A special circuit is implemented to achieve a joint line free display in SSC mode (e.g. Double Window Display). This circuit synchronizes the two input sources and removes the joint lines by automatic controlled shifting of the display raster phase. This procedure enlarges the value of OPDELM resulting in an delayed start of the output processing.

The I²C Bus parameters RSHFTM and RSHFTS enable joint line free display for master and slave channel, separately. SHFTSTEP fixes the amount of lines which is added to OPDELM with each output frame. The readable I²C Bus parameter SHIFACT signalizes the progressing shifting operation.

It is recommended to enable the registers RSHFTM and RSHFTS in all application modes.

System description

| Mode | Input Master Channel | Input Slave Channel | Output Display Channel | Comment |
|-------------|----------------------|---------------------|------------------------|----------------------------------------------------------------------------------------|
| SRC | 625/50i | 625/50i | 625/100i 625/50p | Motion compensation for master channel possible |
| SRC | 525/60i | 525/60i | 525/120i 525/60p | Motion compensation for master channel possible |
| SRC | 625/50i | 525/60i | 625/100i 625/50p | joint line free display for slave channel possible (NEW) |
| SRC | 525/60i | 625/50i | 525/120i 525/60p | joint line free display for slave channel possible (NEW) |
| SSC/ MUP | 625/50i | 625/50i | 625/100i 625/50p | No motion compensation possible |
| SSC/ MUP | 525/60i | 525/60i | 525/120i 525/60p | No motion compensation possible |
| SSC/ MUP | 625/50i | 525/60i | 625/100i 625/50p | No motion compensation possible, no joint line free display for slave channel possible |
| SSC/ MUP | 525/60i | 625/50i | 525/120i 525/60p | No motion compensation possible, no joint line free display for slave channel possible |

Table 61 Supported data formats

5.6.7 Master slave switch

This chapter describes the I²C Bus parameters used to execute a master and slave exchange.

| I ² C Bus parameter [Default] | Sub address | Description |
|------------------------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MASTSLA [0] | 55h | Master / Slave shift: 1: Master and slave input signals are exchanged, reset of display raster shift 0: Display raster is synchronized to input master channel (vertical sync) |
| MASLSHFT [0] | 56h | Master / Slave shift: 1: Display raster is shifted slave phase to prepare a master/slave switch 0: Display raster is synchronized to input master channel (vertical sync) |

Table 62 Input write I²C Bus parameter

System description

| I ² C Bus parameter [Default] | Sub address | Description |
|------------------------------------------|-------------|----------------------------------------------------------------------------------------------------|
| SHIFACT | 7Fh | Shifting of display raster phase active 1: phase shift in progress 0: phase shift not active |

Table 63 Output read I²C Bus parameter

Master slave exchange means an animated exchange of the master and slave picture source without visible synchronization problems of the deflection PLL compared with a hard switch between both sources. To avoid this synchronization problem the display raster phase is slowly shifted to a position that fits to the slave channel sync pulses. Then the exchange can be done without visible artefacts. For the animation see "**Configuration switch**" on page 65.

What to do to perform a master slave switch:

1. I²C Parameter MASLSHFT must be set. Shift process is started.
2. The I²C output signal SHIFACT must be observed. After setting MASLSHFT is becomes '1' and signalizes that the shift process is active. When it becomes '0' the shift process is finished and the desired phase of the display raster is obtained.
3. At the same time exchanging of master and slave inputs and setting of I²C parameter MASTSLA must be performed. Now the chip is synchronized to the former slave channel that now has become the master.
4. At last the I²C Bus parameters MASLSHFT and MASTSLA should be reset.

5.6.8 Refresh and still picture mode

The master and the slave channel picture can be frozen by the I²C Bus parameter FREEZEM and FREEZES, respectively. The I²C Bus parameters REFRON and REFRPER may be used to activate a memory refresh for the internal memory.

System description

| I ² C Bus parameter [Default] | Sub address | Description |
|------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------|
| FREEZEM [0] | 58h | Freeze picture master 1: freezed (no writing of master channel) 0: live |
| FREEZES [0] | 57h | Freeze picture slave 1: freezed (no writing of slave channel) 0: live |
| REFRPER [00] | 53h | Refresh period of the memory (REFRON=1; 50 Hz, 625 lines standard) 00: ~ 10ms 01: ~ 7ms 10: ~ 5.5ms 11: ~ 4ms |
| REFRON [0] | 55h | Refresh of internal memory 1: memory refresh activated 0: no memory refresh |

Table 64 Input write I²C Bus parameter

5.6.9 Memory management and animation controlling

The "Example for animation" on page 75 shows a possible application of the SDA 9415. 11 still pictures plus one life picture (cup of coffee) are located around a second life (boat) picture (see picture number 1). The still pictures plus one life picture (cup of coffee) are located in the slave memory and the life picture (boat) in the master memory. The user wants to switch now between the cup of coffee and the boat channel. A possible animation could look like this. The boat will be compressed and disappears (number 2 and number 3). Due to the fact, that only background colour should be visible, the parts of the life picture, which disappear after compression, will be overwritten with the back ground colour. Afterwards the new channel is expanded and overwrites the border colour (cup of coffee, number 4 and number 5).

To support this and other features several I²C Bus parameters exists, which will be described in more detail afterwards.

System description

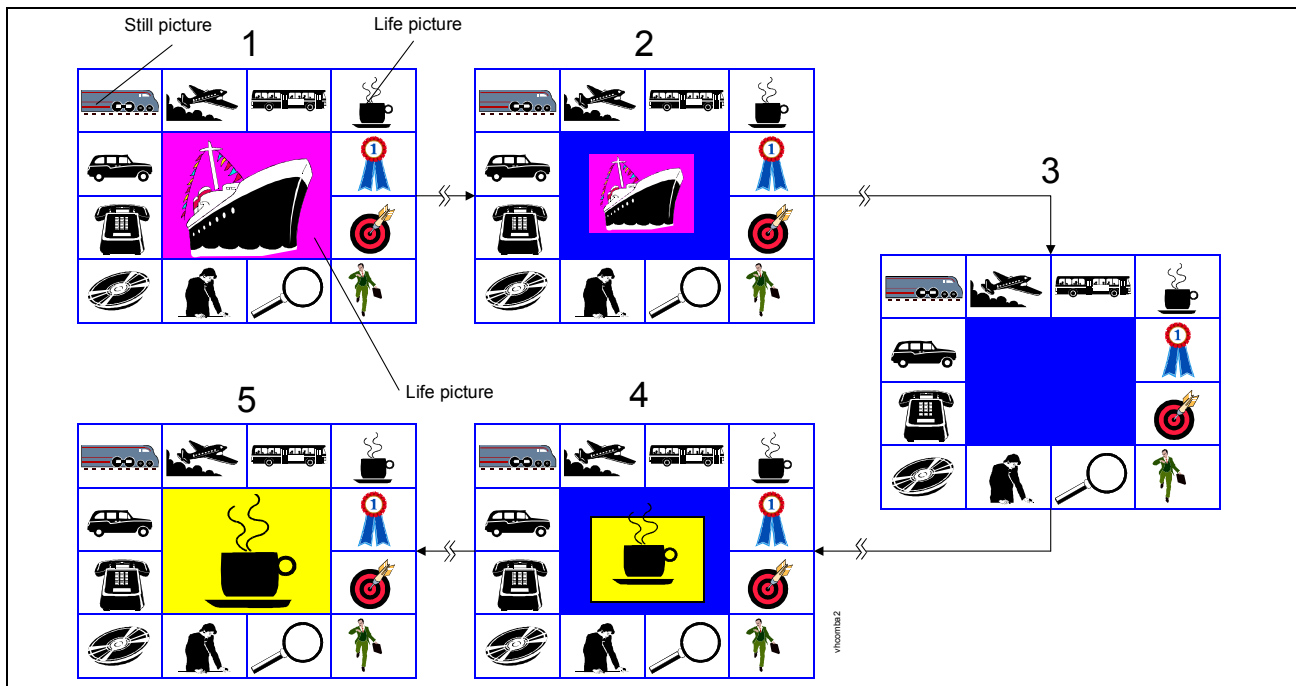


Figure 29 Example for animation

The I²C Bus parameters IPOSXM and IPOSYM or IPOSXS and IPOSYS, respectively, specify the position of the left upper corner of a stored picture. The figure below explains the functionality of the I²C Bus parameters. The whole memory is organized as blocks, which have a width of 32 pixels. The position (x,y) defined by the I²C Bus parameters is defined by the equation below:

$$(x, y) = \left(32 \cdot \left(\frac{IPOSXM}{8} \right) + 4 \cdot (IPOSXM \text{ modulo } 8), IPOSYM \right)$$

Figure 30 Equation of the position of the left upper picture corner

The IPOSYM and IPOSYS I²C Bus parameter specify the vertical position with a resolution of one line for 4:1:1 format and 2 lines for 4:2:0 format for the master and slave channel, respectively. The 5 MSBs of the IPOSXM and IPOSXS defines the horizontal position with a resolution of 32 pixels (block resolution). The 3 LSBs of IPOSXM and IPOSXS are used for fine positioning of the picture in a block with a resolution of 4 pixels. Due to the fact, that only blocks can be written to the memory, the pixels left of the fine positioning are filled up with border values (border values are defined by YBORDERM/YBORDERS, UBORDERM/UBORDERS, VBORDERM/VBORDERS). If the number of pixels is smaller as 32 pixels (block size), the missing pixels of a block are also filled up with border values.

System description

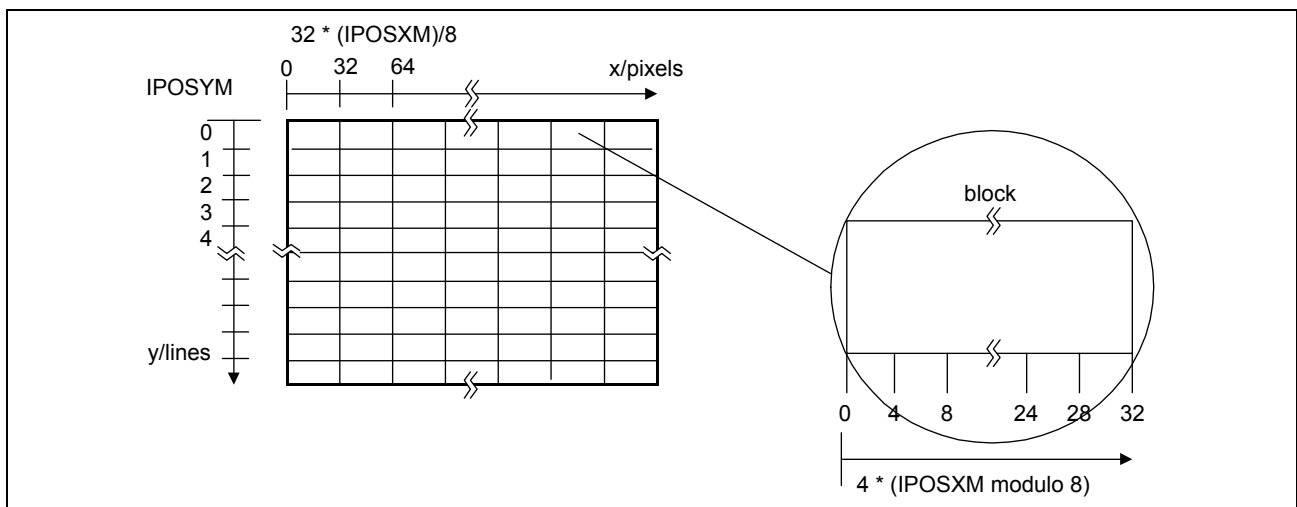


Figure 31 Explanation of memory management I

The **Figure 32** shows a picture (boat, number 1), which is located with the left upper corner at the position (x1,y1). The picture will be compressed in vertical and horizontal direction and stored at the position (x2,y2). The vertical and horizontal compression mechanism of the input signal was explained before (compare "**Vertical and horizontal compression (VHCOMM/VHCOMS)**" on page 36). This result could look like as showed in the picture number 2b. Parts of the original boat are still visible. Therefore in addition the I²C Bus parameters LEBORDM/LEBORDS, RIBORDM/RIBORDS, UPBORDM/UPBORDS and LWBORDM/LWBORDS exist. These I²C Bus parameters specify the amount of pixels at the left side and the right side and the amount of lines at the top and the bottom which has to be written in addition into the memory with coloured border values (I²C Bus parameters YBORDERM, YBORDERS, UBORDERM, UBORDERS, VBORDERM, VBORDERS). Then the result could look like as showed in the picture number 2a (white border colour). The amount of pixels at the left side can be defined by the I²C Bus parameters LEBORDM/LEBORDS (amount of border pixels = 4 * LEBORDM/LEBORDS) and the amount of pixels at the right side can be defined by the I²C Bus parameter RIBORDM/RIBORDS (amount of border pixels = 4 * RIBORDM/RIBORDS). The maximum amount of pixels, which can be written in addition, is 28 pixels on each side. The I²C Bus parameters UPBORDM/S and LWBORDM/S specify the amount of lines which has to be written in addition into the memory at the upper and lower edge of the picture with coloured border values. The maximum amount of lines, which can be written in addition, is 15 on each side. But there is a limitation that the sum of UPBORDM/UPBORDS + LWBORDM/LWBORDS should not exceed 20 (PAL) lines. In horizontal direction as mentioned before only blocks (32 pixels) can be written into the memory. That means for instance if the LEBORDM parameter has a value bigger as zero and the 3 LSBs of IPOSXM parameter are zero (start position at a begin of a block), that the complete block on the left side of the block specified by IPOSXM will be filled with border colour.

System description

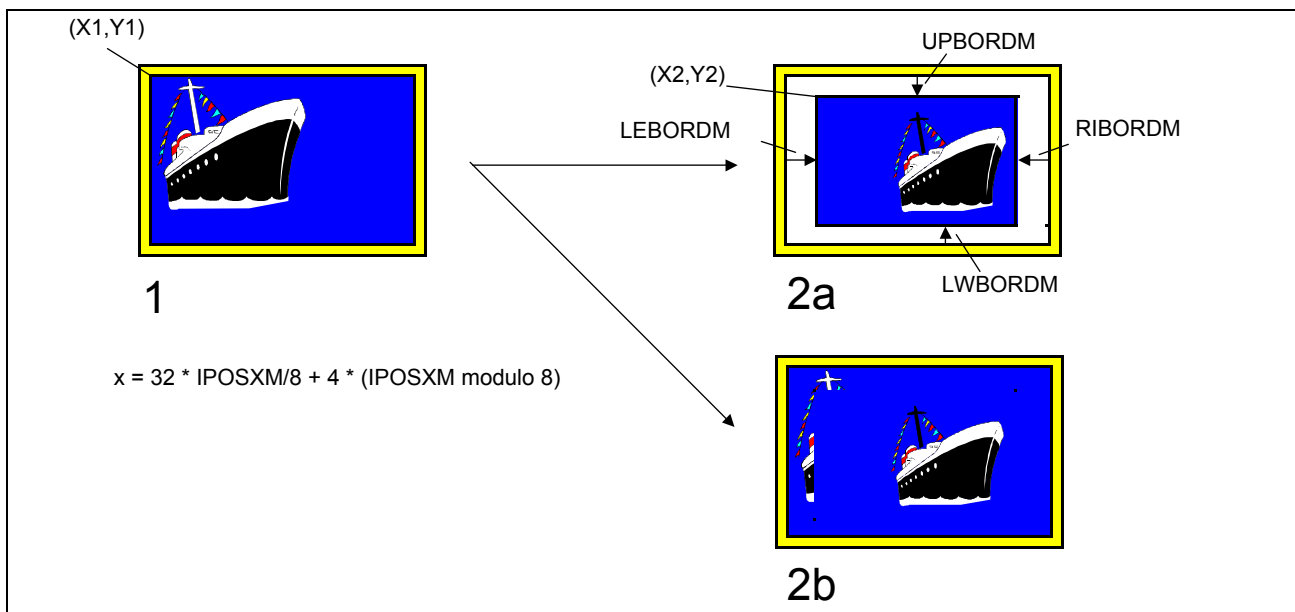


Figure 32 Explanation of memory management II

So the animation shown in the **Figure 32** can be done in the following way. The picture (boat) has at the beginning a defined size (defined by the I²C Bus parameters APPLM1, ALPFM1, INTHM1, DEZHM1, INTVM1, DEZVM1) and the left upper corner of the picture is located at the position (x1,y1) (defined by IPOSXM1, IPOSYM1). Specify the new picture size. Set the corresponding I²C Bus parameters (APPLM2, ALPFM2, INTHM2, DEZHM2, INTVM2, DEZVM2) to get the new picture size. Specify the new vertical and horizontal position (x2,y2) (defined by IPOSXM2, IPOSYM2). Specify in addition the amount of lines at the upper and lower edge, which has to be overwritten with border values. In addition the amount of pixels at the left and right edge, which has to be overwritten with border values (LWBORDM, UPBORDM, LEBORDM, RIBORDM). Send the new values to the I²C interface. Remember that the reduction of the picture is limited in horizontal and vertical direction, if the border should be overwritten with border colour.

The **Figure 33** shows in detail what happens by means of a horizontal bar, which is horizontally reduced. The width of the bar is 84 pixels (compare **Figure 33**). The position x1, defined by IPOSX1 is for instance,

$$IPOSXM1=00001100b=12 \Rightarrow x1 = 32 * 1 + 4 * 4 = 48$$

The I²C Bus parameters LEBORDM and RIBORDM are both equal 0. The first block and the last block are filled up with border values (black colour - background value).

The bar is compressed horizontally and the new width of the bar is 44 pixels. The new position defined by IPOSX2 after the reduction step may be

$$IPOSXM2=00010001b=17 \Rightarrow x2 = 32 * 2 + 4 * 1 = 68.$$

That means the actual picture size is reduced for 40 pixels, 20 pixels at the left side (Left Side = 68 - 48 = 20) and 20 pixels at the right side (Right Side = 132 - 20). Therefore the

System description

I²C Bus parameter LEBORDM has to be set to LEBORDM=5 (amount of pixels = 4*LEBORDM = 4*5 = 20), if the pixels remaining in the memory should be overwritten with border values. In addition the I²C Bus parameter RIBORDM has to be set to RIBORDM=5 (amount of pixels = 4*RIBORDM = 4*5 = 20), if the pixels remaining in the memory should be overwritten with border values. The new position of the left edge is 68 and begin of the block is 64, thus the difference between the begin of the bar and the actual block is 68-64=4. That means that from the additional 20 pixels, which have to be written left of the bar, at least 16 pixels belong to the block which begins at the position 32. That means, that the complete block (begin at position 32) is filled up with border values. The same argumentation is valid for the right edge of the bar.

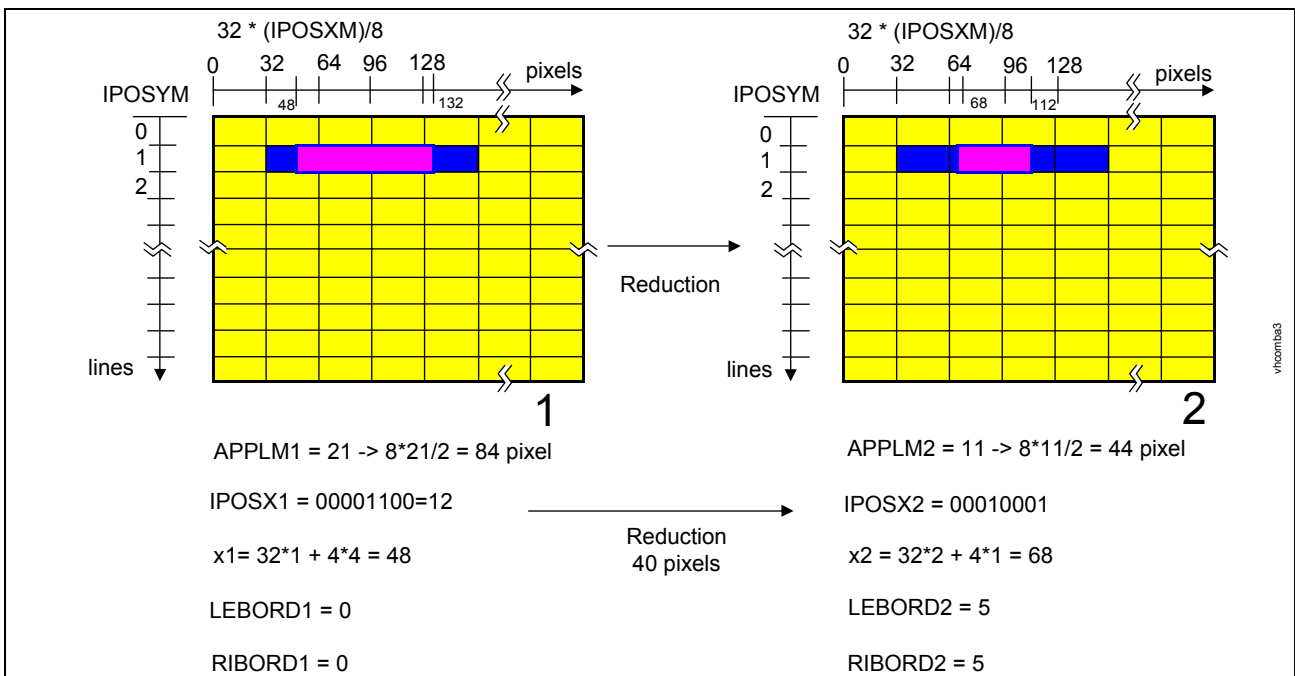


Figure 33 Explanation of memory management III

Repeating the procedure described above must be used for an animation as explained in **Figure 29**.

System description

| I²C Bus parameter [Default] | Sub address | Description |
|-----------------------------------------------|--------------------|----------------------------------------------------------------|
| UPBORDM [0] | 06h | Amount of upper border lines by vertical compression master |
| LWBORDM [0] | 06h | Amount of lower border lines by vertical compression master |
| LEBORDM [0] | 03h | Amount of left border pixels by horizontal compression master |
| RIBORDM [0] | 03h | Amount of right border pixels by horizontal compression master |
| UPBORDS [0] | 28h | Amount of upper border lines by vertical compression slave |
| LWBORDS [0] | 28h | Amount of lower border lines by vertical compression slave |
| LEBORDS [0] | 25h | Amount of left border pixels by horizontal compression slave |
| RIBORDS [0] | 25h | Amount of right border pixels by horizontal compression slave |
| IPOSXM [0] | 02h | Horizontal picture position in the memory for master |
| IPOSXS [0] | 24h | Horizontal picture position in the memory for slave |
| IPOSYM [0] | 01h | Vertical Picture Position in the Memory for master |
| IPOSYS [0] | 23h | Vertical Picture Position in the Memory for slave |

Table 65 Input write I²C Bus parameter

It is possible to write border colours instead of the master or slave channel in different areas. Therefore the I²C parameters FORCOLM and FORCOLS can be used.

System description

| I ² C Bus parameter [Default] | Sub address | Description |
|------------------------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------|
| YBORDERM [0001] | 04h | Y border value (Yborder(3) Yborder(2) Yborder(1) Yborder(0) 0 0 0 0 = 00010000 = 16), YBORDERM defines the 4 MSB's of a 8 bit value |
| UBORDERM [1000] | 05h | U border value (Uborder(3) Uborder(2) Uborder(1) Uborder(0) 0 0 0 0 = 10000000 = 128), UBORDERM defines the 4 MSB's of a 8 bit value |
| VBORDERM [1000] | 05h | V border value (Vborder(3) Vborder(2) Vborder(1) Vborder(0) 0 0 0 0 = 10000000 = 128), VBORDERM defines the 4 MSB's of a 8 bit value |
| YBORDERS [0001] | 26h | Y border value (Yborder(3) Yborder(2) Yborder(1) Yborder(0) 0 0 0 0 = 00010000 = 16), YBORDERS defines the 4 MSB's of a 8 bit value |
| UBORDERS [1000] | 27h | U border value (Uborder(3) Uborder(2) Uborder(1) Uborder(0) 0 0 0 0 = 10000000 = 128), UBORDERS defines the 4 MSB's of a 8 bit value |
| VBORDERS [1000] | 27h | V border value (Vborder(3) Vborder(2) Vborder(1) Vborder(0) 0 0 0 0 = 10000000 = 128), VBORDERS defines the 4 MSB's of a 8 bit value |
| FORCOLM [0] | 04h | Force colour master channel 1: on 0: off |
| FORCOLS [0] | 26h | Force colour slave channel 1: on 0: off |

Table 66 Input write I²C Bus parameter

5.7 Output sync controller (OSCM/S)

| Signals | Pin number | Description |
|------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| HOUT | 4 | horizontal synchronization signal (polarity programmable, I ² C Bus parameter 4Ah HOUTPOL, default: high active) |
| VOUT | 5 | vertical synchronization signal (polarity programmable, I ² C Bus parameter 4Ah VOUTPOL, default: high active) |
| BLANK | 7 | free programmable horizontal blanking signal (polarity programmable, I ² C Bus parameter 49h BLANKPOL, default: high active) |
| INTERLACED | 6 | interlaced signal (can be used for AC coupled deflection circuits) |

Table 67 Output signals

The output sync controller generates horizontal and vertical synchronization signals for the scan rate converted output signal. The figure below shows the block diagram of the OSCM/S and the existing I²C Bus parameters.

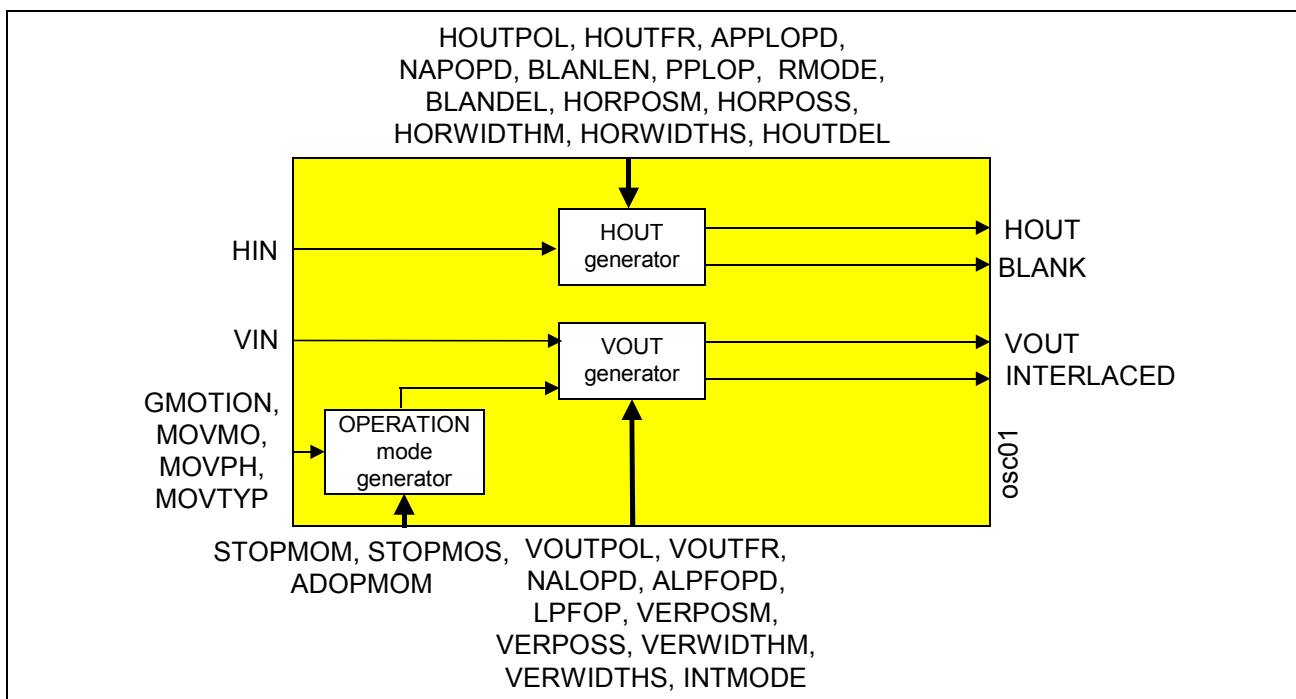


Figure 34 Block diagram of OSCM/S

Furthermore the output sync controller derives framing signals from the generated HOUT and VOUT for the output data processing. The framing signals depend on different I²C Bus parameters. The whole output picture is a combination of three channels:

- 1: Background channel
- 2: Output channel master
- 3: Output channel slave

The background channel has always the lowest priority. The priority between output channel master and slave is defined by an I²C Bus parameter PRIORMS. The figure below shows an example for the combination of the three channels. The background colour black has lowest priority. The picture content of master channel is a phone and the picture content of slave channel is a airplane. In this case the slave channel has the highest priority. To enable or disable the display of the master or slave channel the I²C parameters MASTERON and SLAVEON can be used.

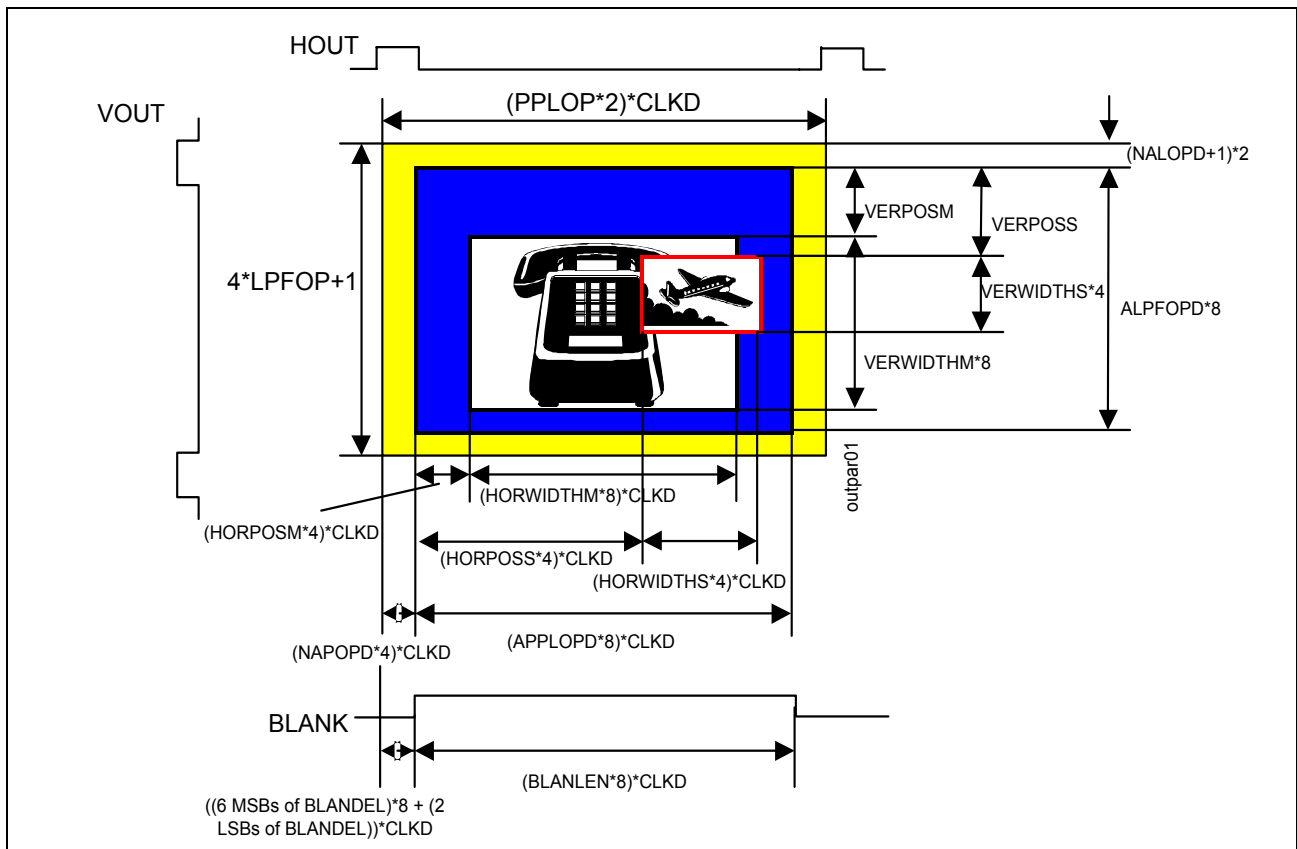


Figure 35 Output I²C Bus parameter

| I ² C Bus parameter [Default value] | Sub address | Description |
|---------------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NALOPD [22] | 36h | Not Active Line OutPut Display defines the number of lines from the V-Sync to the first active line of the output frame |
| ALPFOPD [144] | 37h | Active Lines Per Field OutPut Display defines the number of active lines per output frame |
| VERPOSM [0] | 3Ch | VERTical POSition Master defines the number of lines from the first active line of the background channel to the first active line of the master channel |
| VERWIDTHM [72] | 40h | VERTical WIDTH Master defines the number of active lines of the master channel per output frame |
| VERPOSS [0] | 3Dh | VERTical POSition Slave defines the number of lines from the first active line of the background channel to the first active line of the slave channel |
| VERWIDTHS [144] | 41h | VERTical WIDTH Slave defines the number of active lines of the slave channel per output frame |
| LPFOP [156] | 38h | Lines Per Frame OutPut defines the number of lines per output frame (only valid for VOUTFR=1) |
| NAPOPD [0] | 39h | Not Active Pixel OutPut Display defines the number of pixels from the H-Sync to the first active pixel |
| APPLOPD [90] | 43h | Active Pixels Per Line OutPut Display defines the number of pixels per line (background, master and slave channel) |
| HORPOSM [0] | 3Ah | HORizontal POSition Master defines the number of pixels from the first active pixel of the background channel to the first active pixel of the master channel |
| HORWIDTHM [90] | 3Eh | HORizontal WIDTH Master defines the number of active pixels of the master channel |
| HORPOSS [0] | 3Bh | HORizontal POSition Slave defines the number of pixels from the first active pixel of the background channel to the first active pixel of the slave channel |
| HORWIDTHS [180] | 3Fh | HORizontal WIDTH Slave defines the number of active pixels of the slave channel |
| PPLOP [432] | 45h, 46h | Pixel Per Line OutPut defines the number of pixels between two consecutive H-Syncs (only valid for HOUTFR=1) |
| BLANDEL [0] | 42h | BLANK DELay defines the distance from the H-Sync to the active edge of the BLANK signal in number of CLKD clocks |
| BLANLEN [180] | 44h | BLANK LENgth defines the length of the BLANK signal in number of CLKD clocks |
| HOUTDEL [0] | 35h | Horizontal delay of HOUT and VOUT signal in clocks of CLKD |
| PRIORMS [1] | 43h | Priority of master or slave channel: 1: master channel priority 0: slave channel priority (SFCPR should be fixed to V_{SS}). |

| I ² C Bus parameter [Default value] | Sub address | Description |
|---------------------------------------------------|-------------|---------------------------------------------------------|
| MASTERON [1] | 53h | Display of master channel: 1: enabled 0: disabled |
| SLAVEON [0] | 53h | Display of slave channel: 1: enabled 0: disabled |

Figure 36 Output write I²C Bus parameter

The next paragraphs describe the HOUT and VOUT generator in more detail. Both generators have a so called “locked-mode” and “freerunning-mode”. Not all combinations of the modi make sense. The table below shows ingenious configurations.

| Mode | HOUTFR | VOUTFR | CLKMDEN |
|--------------------------|--------|--------|---------|
| “H-and-V-locked” | 0 | 0 | 0 |
| “H-freerunning-V-locked” | 1 | 0 | 1 |
| “H-and-V-freerunning” | 1 | 1 | 1 |

Figure 37 Ingenious configurations of the HOUT and VOUT generator

5.7.1 HOUT generator

The HOUT generator has two operation modes, which can be selected by the I²C Bus parameter HOUTFR. The HOUT signal is active high (HOUTPOL=0) for 64 clock cycles (X1/CLKD). In the freerunning-mode the HOUT signal is generated depending on the PPLOP I²C Bus parameter. In the locked-mode the HOUT signal is locked on the incoming H-Sync signal HIN. The polarity of the HOUT signal is programmable by the I²C Bus parameter HOUTPOL. The BLANK signal can be used to mark the active part of a line. To avoid transition artifacts of digital filters the number of active pixels can be symmetrically reduced using the CAPPM and CAPPS I²C Bus parameter.

| I ² C Bus parameter | Sub address | Description |
|-------------------------------------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------|
| HOUTFR 1: free run 0: locked mode | 4Ah | HOUT generator mode select |
| CAPPM 00: k = 0 01: k = 8 10: k = 16 11: k = 24 | 46h | Reducing factor for the HORIZONTAL WIDTH Master value of the master channel Number of active pixels per line = 8 * HORWIDTHM - 2*k |
| CAPPS 00: k = 0 01: k = 8 10: k = 16 11: k = 24 | 46h | Reducing factor for the HORIZONTAL WIDTH Slave value of the master channel Number of active pixels per line = 8 * HORWIDTHM - 2*k |

Table 68 Output write I²C Bus parameter

5.7.2 VOUT generator

The VOUT generator has two operation modes, which can be selected by the I²C Bus parameter VOUTFR. The VOUT signal is active high (VOUTPOL=0) for two output lines. In the freerunning-mode the VOUT signal is generated depending on the LPFOP I²C Bus parameter.

In the locked-mode the VOUT signal is synchronized by the incoming V-Sync signal VIN (means the internal VIN delayed by the I²C Bus parameter OPDELM, compare "**Input sync controller (ISCM/ISCS)**" on page 26). The RMODE I²C Bus parameter (line-scanning pattern mode 1: progressive, 0: interlaced) determines the scan rate conversion mode. If RMODE=1, then for each incoming V-sync signal VIN an outgoing V-sync signal VOUT has to be generated (e.g. 50 Hz interlaced to 50 Hz progressive scan rate conversion). If RMODE=0, then during one incoming V-Sync signal, two VOUT pulses have to be generated (e.g. 50 Hz interlaced to 100 Hz interlaced scan rate conversion).

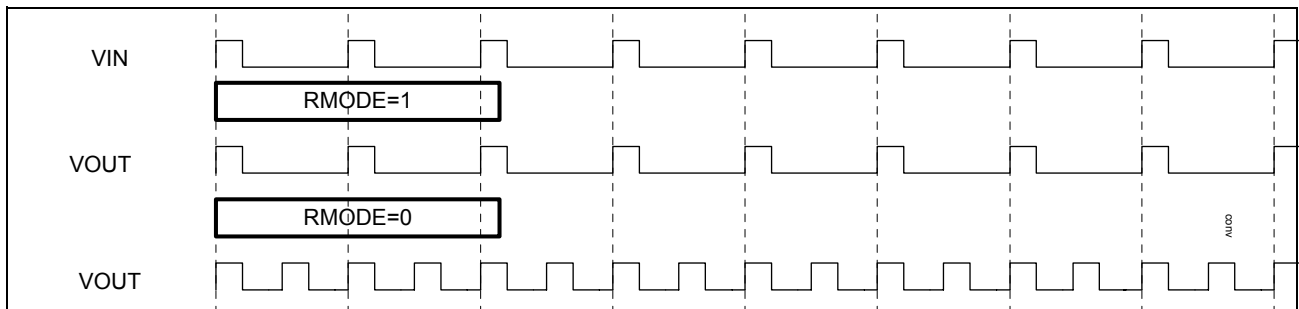


Figure 38 VOUT generation depending on I²C Bus parameter RMODE

The polarity of the VOUT signal is programmable by the I²C Bus parameter VOUTPOL. The VOUT signal has a delay of two CLKOUT clocks to the HOUT signal or in case of interlaced a delay of a half line plus two CLKOUT clocks.

The INTERLACED signal can be used for AC-coupled deflections. Depending on the I²C Bus parameter INTMODE the value of this signal will be generated. The **Table 69** shows the definition of this signal (compare "**Operation mode generator**" on page 87).

| | output field phase 0 | output field phase 1 | output field phase 2/0 | output field phase 3/1 |
|---------|----------------------|----------------------|------------------------|------------------------|
| INTMODE | INTMODE(0) | INTMODE(1) | INTMODE(2) | INTMODE(3) |

Table 69 Output write I²C Bus parameter INTMODE

| I ² C Bus parameter | Sub address | Description |
|------------------------------------------|-------------|----------------------------------------------------------------------|
| VOUTFR 1: free run 0: locked mode | 4Ah | VOUT generator mode select |
| RMODE 1: progressive 0: interlaced | 48h | line-scanning pattern mode |
| INTMODE | 49h | Free programmable INTERLACED signal for AC-coupled deflection stages |

Table 70 Output write I²C Bus parameter INTMODE

5.7.3 Switching from H-and-V-freerunning to H-and-V-locked mode

In H-and-V-freerunning mode, generally, the phase of the generated synchronization line-scanning pattern has no correlation to the input line-scanning pattern. A hard switch from the H-and-V-freerunning mode to the H-and-V-locked mode therefore would cause visible synchronization artefacts. To avoid these problems the SDA 9415 enlarges the line and the field lengths of the output sync signals HOUT and VOUT in a defined procedure to enable an invisible synchronization of the freerunning output to the input.

For vertical synchronization the maximum synchronization time is 260 ms for interlaced and 520 ms for progressive display modes. Horizontal synchronization is performed in a maximum time of 50 ms. To get the best performance it is recommended to change at first the vertical and after the mentioned delay times the horizontal mode from free running to locked.

5.7.4 Operation mode generator

The VOUT generator determines the VOUT signal. For proper operation of the VOUT generator information about the line-scanning pattern sequence is necessary. The I²C Bus parameters STOPMOM (STatic OPeration MOde Master), STOPMOS (STatic OPeration MOde Slave) and the I²C Bus parameter ADOPMOM (ADaptive OPeration MOde Master) define the line-scanning pattern sequence and the scan rate conversion algorithms.

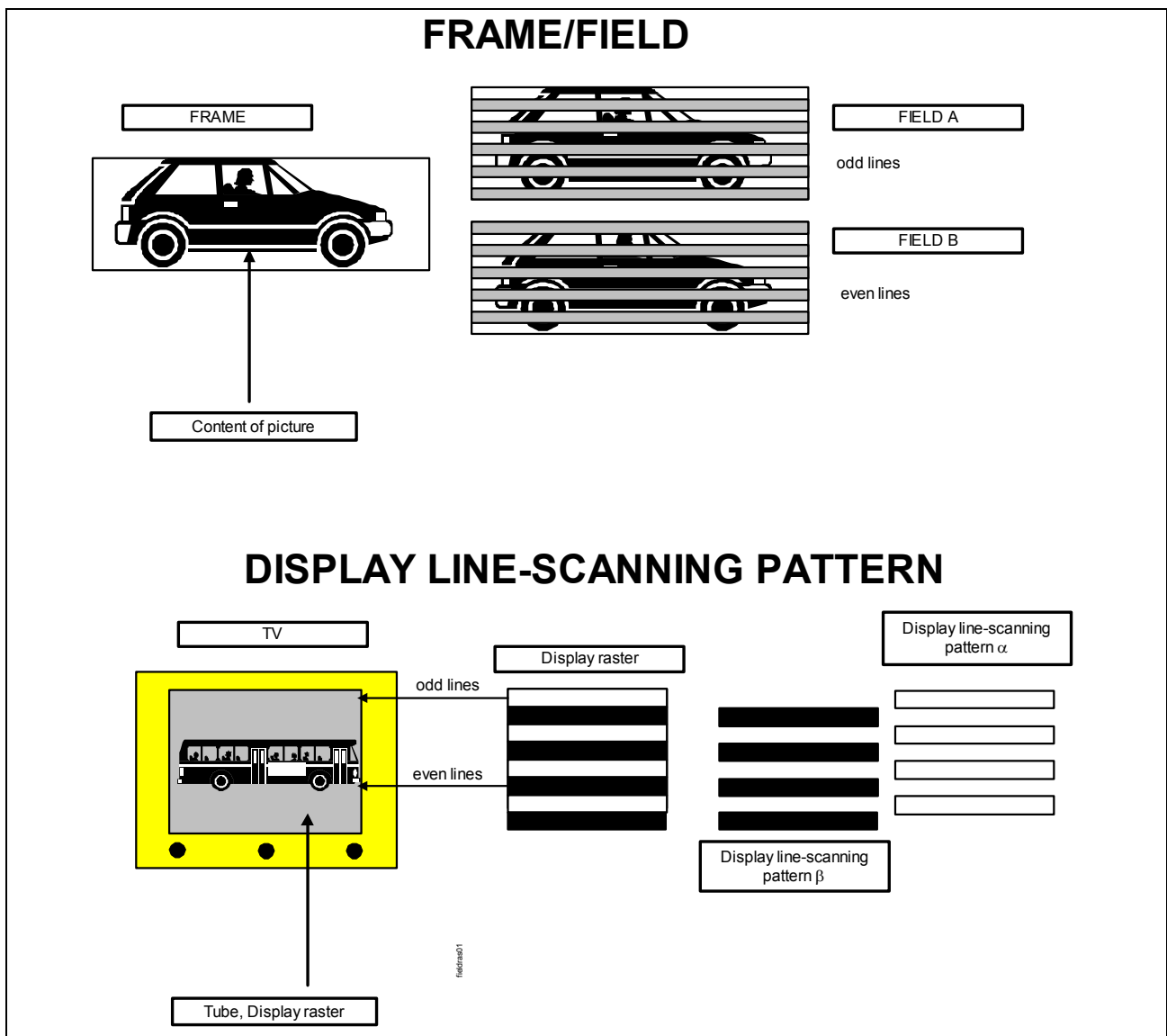


Figure 39 Explanation of field and display line-scanning pattern

The interlaced input signal (e.g. 50 Hz PAL or 60 Hz NTSC) is composed of a field A (odd lines) and a field B (even lines).

A^n - Input signal, field A at time n,

B^n - Input signal, field B at time n

The field information describes the picture content. The output signal, which could contain different picture contents (e.g. field A, field B) can be displayed with the display line-scanning pattern α or β .

(A^n, α) - Output signal, field A at time n, displayed as line-scanning pattern α ,

(A^n, β) - Output signal, field A at time n, displayed as line-scanning pattern β ,

$((A^*)^n, \beta)$ - Output signal, field A line-scanning pattern interpolated into field B at time n, displayed as line-scanning pattern β

$(A^n B^{n-1}, \alpha+\beta)$ - Output signal, frame AB at time n, progressive

The table below describes the different scan rate conversion algorithms and the corresponding line-scanning pattern sequences. The delay between the input field and the corresponding output fields depends on the OPDELM parameter and the default value for the delay is an half input field.

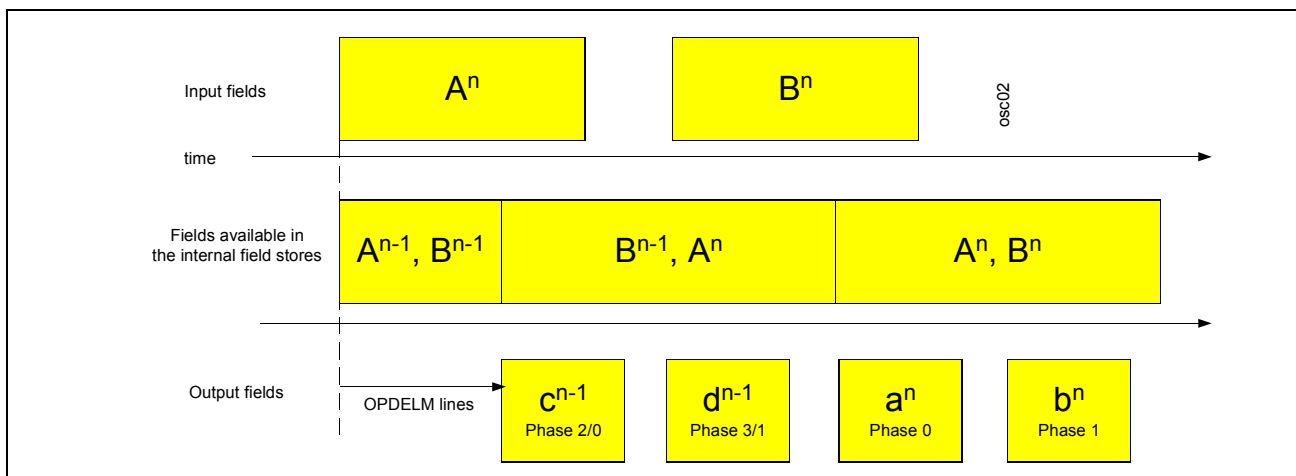


Figure 40 Explanation of operation mode timing

| STOP-MOM | Scan rate conversion algorithm | Input field A | | Input field B | |
|----------|--------------------------------|-------------------------|--------------------------|---------------------------|---------------------------|
| | | Output field an phase 0 | Output field bn phase 1 | Output field cn phase 2/0 | Output field dn phase 3/1 |
| 0000 | VDU, camera mode | $p(c)^*$, α | $p(d)$, β | $p(a)$, α | $p(b)$, β |
| 0001 | VDU, film mode, phase 0, PAL | $p(mc)$, α | $p(md)$, β | $p(ma)$, α | $p(mb)$, β |
| 0010 | VDU, film mode, phase 1, PAL | $p(ma)$, α | $p(mb)$, β | $p(mc)$, α | $p(md)$, β |
| 0011 | Frame repetition, ABAB | A^n , α | B^{n-1} , β | A^n , α | B^n , β |
| 0100 | FRAME repetition, BABA | B^{n-1} , β | A^n , α | B^n , β | A^n , α |
| 0101 | Simple 100, AABB | A^n , α | A^n , α | B^n , β | B^n , β |
| 0110 | Simple 100, BBAA | B^{n-1} , β | B^{n-1} , β | A^n , α | A^n , α |
| 0111 | Field repetition, AAAA I | A^n , α | A^n , β | A^n , α | A^n , β |
| 1000 | Field repetition, AAAA II | A^n , α | A^n , α | A^n , α | A^n , α |
| 1001 | Field repetition, BBBB I | B^{n-1} , α | B^{n-1} , β | B^n , α | B^n , β |
| 1010 | Field repetition, BBBB II | B^{n-1} , β | B^{n-1} , β | B^n , β | B^n , β |
| 1100 | Simple 100, AA*B*B | A^n , α | $(A^*)^n$, β | $(B^*)^n$, α | B^n , β |
| 1101 | Simple 100, BB*A*A | B^{n-1} , β | $(B^*)^{n-1}$, α | $(A^*)^n$, β | A^n , α |
| 1110 | VDU, film mode, phase 0, NTSC | $p(ma)$, α | $p(mb)$, β | $p(ma)$, α | $p(mb)$, β |
| 1111 | VDU, film mode, phase 1, NTSC | $p(mc)$, α | $p(md)$, β | $p(mnc)$, α | $p(mnd)$, β |

Table 71 Static operation modes (only valid for ADOPMOM=0, RMODE=0)

*) $p(a)$: a field - motion compensated; $p(b)$: b field - motion compensated

$p(c)$: c field - motion compensated; $p(d)$: d field - motion compensated

$p(ma)$: a field - motion compensated film mode; $p(mb)$: b field - motion compensated film mode

$p(mc)$: c field - motion compensated film mode; $p(md)$: d field - motion compensated film mode

$p(mnc)$: c field - motion compensated film mode for NTSC

$p(mnd)$: d field - motion compensated film mode for NTSC

| STOPMOM | Scan rate conversion algorithm | Input field A | Input field B |
|---------|--------------------------------|---------------------------------------|---------------------------------------|
| | | Output field phase 0 | Output field phase 2/0 |
| 0000 | VDU, camera mode | $p(cd)^*, \alpha+\beta$ | $p(ab), \alpha+\beta$ |
| 0001 | VDU, film mode, phase 0, PAL | $p(mcd), \alpha+\beta$ | $p(mab), \alpha+\beta$ |
| 0010 | VDU, film mode, phase 1, PAL | $p(mab), \alpha+\beta$ | $p(mcd), \alpha+\beta$ |
| 0011 | Frame repetition, AB | $(A^n B^{n-1}), \alpha+\beta$ | $(A^n B^n), \alpha+\beta$ |
| 0100 | Frame repetition, AB median | $(A^n (B^*)^{n-1}), \alpha+\beta$ | $((A^*)^n B^n), \alpha+\beta$ |
| 0101 | Simple 50, AA*, B*B | $(A^n (A^*)^n), \alpha+\beta$ | $((B^*)^n B^n), \alpha+\beta$ |
| 1100 | Field repetition, AA* | $(A^n (A^*)^n), \alpha+\beta$ | $(A^n (A^*)^n), \alpha+\beta$ |
| 1101 | Field repetition, BB* | $((B^*)^{n-1} B^{n-1}), \alpha+\beta$ | $((B^*)^{n-1} B^{n-1}), \alpha+\beta$ |
| 1110 | VDU, film mode, phase 0, NTSC | $p(mab), \alpha+\beta$ | $p(mab), \alpha+\beta$ |
| 1111 | VDU, film mode, phase 1, NTSC | $p(mcd), \alpha+\beta$ | $p(mnc), \alpha+\beta$ |

Table 72 Static operation modes (only valid for ADOPMOM=0, RMODE=1)

- *) $p(ab)$: a+b field - motion compensated
 $p(cd)$: c+d field - motion compensated
 $p(mab)$: a+b field - motion compensated film mode
 $p(mcd)$: c+d field - motion compensated film mode
 $p(mnc)$: c field - motion compensated film mode for NTSC

For STOPMOM=0000 (Micronas VDU) the high performance motion compensation algorithm is used for scan rate conversion which results in a high performance line flicker reduction, double contour elimination and perfect motion display.

The table **Table 73 "Special combinations of STOPMOM and ADOPMOM"** on **page 92** explains some important combinations of both registers. It is possible to force some modes like VDU CAMERA, VDU PAL film mode and VDU NTSC film mode with manual or automatic phase detection in case of film mode.

| STOPMOM | ADOPMOM | Description |
|---------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0000 | 000 | force VDU CAMERA mode |
| 0001 | 000 | force VDU PAL film mode Phase 0 |
| 0010 | 000 | force VDU PAL film mode Phase 1 |
| 0001 | 100 | force VDU PAL with automatic phase detection; PAL film mode is set only once, if it is detected; after that it will be fixed until another mode is selected from the user; STOPMOM 0001 or 0010 is selected automatically |
| 0010 | 100 | same as STOPMOM 0001 and ADOPMOM 100 |
| 1110 | 100 | force VDU NTSC film mode with automatic phase detection; NTSC film mode is set only once, if it is detected; after that it will be fixed until another mode is selected from the user; STOPMOM 1110 and STOPMOM 1111 is selected automatically |
| 1111 | 100 | same as STOPMOM 1110 and ADOPMOM 100 |
| 0001 | 101 | force VDU PAL with automatic phase detection; PAL film mode is set only once, if it is detected; after that it will be fixed until another mode is selected from the user; in addition STOPMOM 0011 will be selected if GMOTION is zero; STOPMOM 0001 or 0010 or 0011 is selected automatically |
| 0010 | 101 | same as STOPMOM 0001 and ADOPMOM 101 |
| 1110 | 101 | force VDU NTSC film mode with automatic phase detection; NTSC film mode is set only once, if it is detected; after that it will be fixed until another mode is selected from the user; in addition STOPMOM 0011 will be selected if GMOTION is zero; STOPMOM 1110 or STOPMOM 1111 or STOPMOM 0011 is selected automatically |
| 1111 | 101 | same as STOPMOM 1110 and ADOPMOM 101 |

Table 73 Special combinations of STOPMOM and ADOPMOM

The table **Table 74 "Display line-scanning pattern sequence" on page 93** shows all possible display line-scanning pattern sequences for the different static operation modes and the lines per field value between two consecutive output V-Syncs. It is assumed, that in case of freerunning-mode LPFOP=156 and in locked-mode the number of lines of the incoming field is 312.5.

| Display line-scanning pattern sequence | 1. to 2. | 2. to 3. | 3. to 4. | 4. to 5.(1.) |
|----------------------------------------|----------|----------|----------|--------------|
| αααα | 312 | 313 | 312 | 313 |
| αβαβ | 312.5 | 312.5 | 312.5 | 312.5 |
| ββββ | 313 | 312 | 313 | 312 |
| βαβα | 312.5 | 312.5 | 312.5 | 312.5 |
| ααββ | 312 | 312.5 | 313 | 312.5 |
| ββαα | 313 | 312.5 | 312 | 312.5 |

Table 74 Display line-scanning pattern sequence

The table below defines the static operation modes for the slave channel. The slave channel is synchronized to the master channel. Therefore only modes with the same output line-scanning pattern as the chosen master channel mode are allowed. Several modes depend on the I²C Bus parameter MEMOP.

| STOPMOS | Scan rate conversion algorithm | allowed for RMODE | allowed output line-scanning pattern | allowed MEMOP |
|---------|--------------------------------------|-------------------|--------------------------------------|---------------|
| 000 | Median, ABAB | 0 | αβαβ, βαβα | 00 SRC |
| 001 | Frame repetition, ABAB | 0 | αβαβ, βαβα | 00 SRC |
| 010 | Simple 100, AABB | 0 | ααββ, ββαα | all |
| 011 | Field repetition, AAAA I | 0 | αβαβ, βαβα | all |
| 100 | Field repetition, AAAA II | 0 | αααα, ββββ | all |
| 101 | Field repetition, BBBB I | 0 | αβαβ, βαβα | all |
| 110 | Field repetition, BBBB II | 0 | αααα, ββββ | all |
| 111 | not defined | 0 | | |
| 000 | Median, AB | 1 | α+β | 00 SRC |
| 001 | Frame repetition, AB | 1 | α+β | 00 SRC |
| 010 | Line doubling, AB | 1 | α+β | all |
| 011 | Line doubling, AA | 1 | α+β | all |
| 100 | Intra field interpolation A+A* | 1 | α+β | 01 SSC |
| 101 | Line doubling, BB | 1 | α+β | all |
| 110 | not defined | 1 | | |
| 111 | Intra field interpolation A+A*, B*+B | 1 | α+β | 01 SSC |

Table 75 Static operation modes slave

The adaptive operation modes (ADOPMOM) define a dynamic switch between different static operation modes controlled by several internal signals. The start point of all modes is the actual chosen STOPMOM as described before. The tables below shows the different adaptive operation modes. The internal used control signals are GMOTION, MOV TYP, MOVMO and MOVPH (compare "**Global motion, film mode and phase detection**" on page 108). Furthermore the internal control signal VTSEQ exists. In case of I²C Bus parameter VCRMODEM=1, VTSEQ is still zero. If VCRMODEM=0, VTSEQ can be equal one (compare "**Input sync controller (ISCM/ISCS)**" on page 26). In this cases the scan rate conversion is forced to a simple field based scan rate conversion algorithm. All internal control signals GMOTION, MOV TYP, MOVMO and MOVPH are also readable by the I²C Bus interface.

Basic adaptive operation modes (RMODE = 0 (interlaced)):

off: ADOPMOM=000/001

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------|------------|
| x | x | x | x | x | STOPMOM | STOPMOS |

VCRMODE off: ADOPMOM=010

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------------------|-----------------------|
| x | x | x | 0 | x | STOPMOM | STOPMOS |
| x | x | x | 1 | x | Simple 100, AABB, 0101 | Simple 100, AABB, 010 |

Still picture mode: ADOPMOM=011

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------------------------|-----------------------|
| x | x | x | 0 | 0 | Frame repetition, ABAB, 0011 | STOPMOS |
| x | x | x | 0 | 1 | STOPMOM | STOPMOS |
| x | x | x | 1 | x | Simple 100, AABB, 0101 | Simple 100, AABB, 010 |

Film mode I; ADOPMOM=100

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|-------------------------------------------|--------------------------|
| 0 | x | x | 0 | x | STOPMOM | STOPMOS |
| 1 | 0 | 0 | 0 | x | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | 0 | 0 | x | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| 1 | 0 | 1 | 0 | x | VDU, film mode, phase 0, NTSC, 1110 | STOPMOS |
| 1 | 1 | 1 | 0 | x | VDU, film mode, phase 1, NTSC, 1111 | STOPMOS |
| x | x | x | 1 | x | Simple 100, AABB, 0101 | Simple 100, AABB, 010 |

Film mode II: ADOPMOM=101

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|-------------------------------------------|--------------------------|
| x | x | x | 0 | 0 | Frame repetition, ABAB, 0011 | STOPMOS |
| 0 | x | x | 0 | 1 | STOPMOM | STOPMOS |
| 1 | 0 | 0 | 0 | 1 | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | 0 | 0 | 1 | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| 1 | 0 | 1 | 0 | 1 | VDU, film mode, phase 0, NTSC, 1110 | STOPMOS |
| 1 | 1 | 1 | 0 | 1 | VDU, film mode, phase 1, NTSC, 1111 | STOPMOS |
| x | x | x | 1 | x | Simple 100, AABB, 0101 | Simple 100, AABB, 010 |

Film mode III: ADOPMOM=110

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------------------------------|-----------------------|
| 0 | x | x | 0 | x | STOPMOM | STOPMOS |
| 1 | 0 | x | 0 | x | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | x | 0 | x | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| x | x | x | 1 | x | Simple 100, AABB, 0101 | Simple 100, AABB, 010 |

Film mode IV: ADOPMOM=111

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------------------------------|-----------------------|
| x | x | x | 0 | 0 | Frame repetition, ABAB, 0011 | STOPMOS |
| 0 | x | x | 0 | 1 | STOPMOM | STOPMOS |
| 1 | 0 | x | 0 | 1 | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | x | 0 | 1 | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| x | x | x | 1 | x | Simple 100, AABB, 0101 | Simple 100, AABB, 010 |

Adaptive operation mode (RMODE = 1 (progressive)):

off: ADOPMOM=000/001

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------|------------|
| x | x | x | x | x | STOPMOM | STOPMOS |

VCRMODE off: ADOPMOM=010

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|-----------------|------------------------|
| x | x | x | 0 | x | STOPMOM | STOPMOS |
| x | x | x | 1 | x | Simple 50, 0101 | Line doubling, AB, 010 |

Still picture mode: ADOPMOM=011

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------------------------|------------------------|
| x | x | x | 0 | 0 | Frame repetition, ABAB, 0011 | STOPMOS |
| x | x | x | 0 | 1 | STOPMOM | STOPMOS |
| x | x | x | 1 | x | Simple 50, 0101 | Line doubling, AB, 010 |

Film mode I: ADOPMOM=100

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|-------------------------------------|------------------------|
| 0 | x | x | 0 | x | STOPMOM | STOPMOS |
| 1 | 0 | 0 | 0 | x | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | 0 | 0 | x | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| 1 | 0 | 1 | 0 | x | VDU, film mode, phase 0, NTSC, 1110 | STOPMOS |
| 1 | 1 | 1 | 0 | x | VDU, film mode, phase 1, NTSC, 1111 | STOPMOS |
| x | x | x | 1 | x | Simple 50, 0101 | Line doubling, AB, 010 |

Film mode II: ADOPMOM=101

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|-------------------------------------|------------------------|
| x | x | x | 0 | 0 | Frame repetition, ABAB, 0011 | STOPMOS |
| 0 | x | x | 0 | 1 | STOPMOM | STOPMOS |
| 1 | 0 | 0 | 0 | 1 | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | 0 | 0 | 1 | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| 1 | 0 | 1 | 0 | 1 | VDU, film mode, phase 0, NTSC, 1110 | STOPMOS |
| 1 | 1 | 1 | 0 | 1 | VDU, film mode, phase 1, NTSC, 1111 | STOPMOS |
| x | x | x | 1 | x | Simple 50, 0101 | Line doubling, AB, 010 |

Film mode III: ADOPMOM=110

| MOVMO | MOVPH | MOV TYP | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------------------------------|------------------------|
| 0 | x | x | 0 | x | STOPMOM | STOPMOS |
| 1 | 0 | x | 0 | x | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | x | 0 | x | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| x | x | x | 1 | x | Simple 50, 0101 | Line doubling, AB, 010 |

Film mode IV: ADOPMOM=111

| MOVMO | MOVPH | MOVTYPE | VTSEQM | GMOTION | STOPMOMint | STOPMOSint |
|-------|-------|---------|--------|---------|------------------------------------|------------------------|
| x | x | x | 0 | 0 | Frame repetition, ABAB, 0011 | STOPMOS |
| 0 | x | x | 0 | 1 | STOPMOM | STOPMOS |
| 1 | 0 | x | 0 | 1 | VDU, film mode, phase 0, PAL, 0001 | STOPMOS |
| 1 | 1 | x | 0 | 1 | VDU, film mode, phase 1, PAL, 0010 | STOPMOS |
| x | x | x | 1 | x | Simple 50, 0101 | Line doubling, AB, 010 |

Table 76 Adaptive operation modes

Example for explanation of the adaptive operation modes:

ADOPMOM = 4: Film mode I, RMODE=0

In this case the scan rate conversion algorithm is controlled by the signal MOVMO, MOVTYPE and MOVPH. If MOVMO is equal 0 the scan rate conversion mode is defined by STOPMOM and STOPMOS (e.g. Micronas VDU). If MOVMO is equal 1 and MOVTYPE is equal 0 the scan rate conversion algorithm is changed depending on the MOVPH signal to Micronas VDU, Film mode, PAL, phase 0 or 1. If MOVMO is equal 1 and MOVTYPE is equal 1 the scan rate conversion algorithm is changed depending on the MOVPH signal to Micronas VDU, Film mode, NTSC, phase 0 or 1. In case of film mode PAL, the MOVPH signal is constant for the applied material. In case of Film mode NTSC, the MOVPH signal changes each 2th or 3th field, respectively.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|---------------------------------|
| STOPMOM | 48h | Static Operation Modes Master |
| STOPMOS | 4Ah | Static Operation Modes Slave |
| ADOPMOM | 49h | Adaptive Operation Modes Master |

Table 77 Output write I²C Bus parameter

5.8 Motion estimation

The 3-D Recursive Search Block-Matching algorithm was introduced as a high performance low-cost motion estimation algorithm suitable for demanding scan rate conversion applications. The figure below explains the principle of the block matching algorithm. The result is a best matching vector, which contains information about velocity and direction of a block at position (x,y).

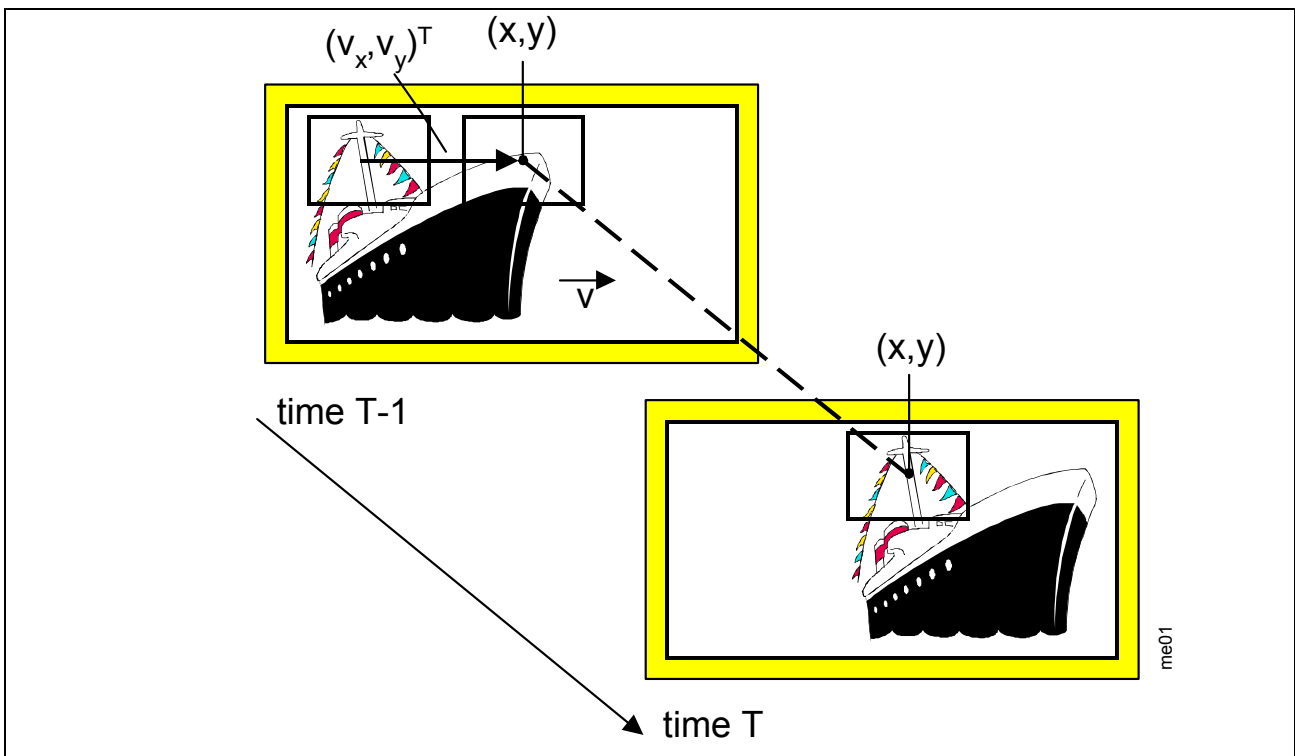


Figure 41 Principle of block matching

The main characteristics of the motion estimator inside of the SDA 9415 are listed in the table below.

| I ² C Bus parameter | | |
|--------------------------------|-------------|-------------------|
| Horizontal range | +/-32 | pels |
| Vertical range | +/-24 | lines |
| Block size | 8x8 (HxV) | pels (frame grid) |
| Accuracy | +/- 1 | pels |
| Candidates | 8 (2x3 + 2) | |
| Amount of blocks | 90*72 (HXV) | |

Table 78 Key I²C Bus parameters of the 3-D RS motion estimation

The **Figure 42** shows the block diagram of the motion estimation and motion compensation block. The field information is read line-wise from the internal field store and written to a line-to-block converter. The motion estimation and the motion compensation block read the field information in parallel block wise from the line-to-block converter. The cache in front of the blocks enables a random access of the field information.

The result of the motion estimation is stored in the vector memory, which is also used as a vector field memory for the 3-D recursive block matching algorithm. At that time only vector information of block resolution is available. The post processing block computes a vector information of pixel resolution basis, which can be used from the motion compensation block for the up conversion process. Finally the results of the motion compensation block are written to the block-to-line converter block.

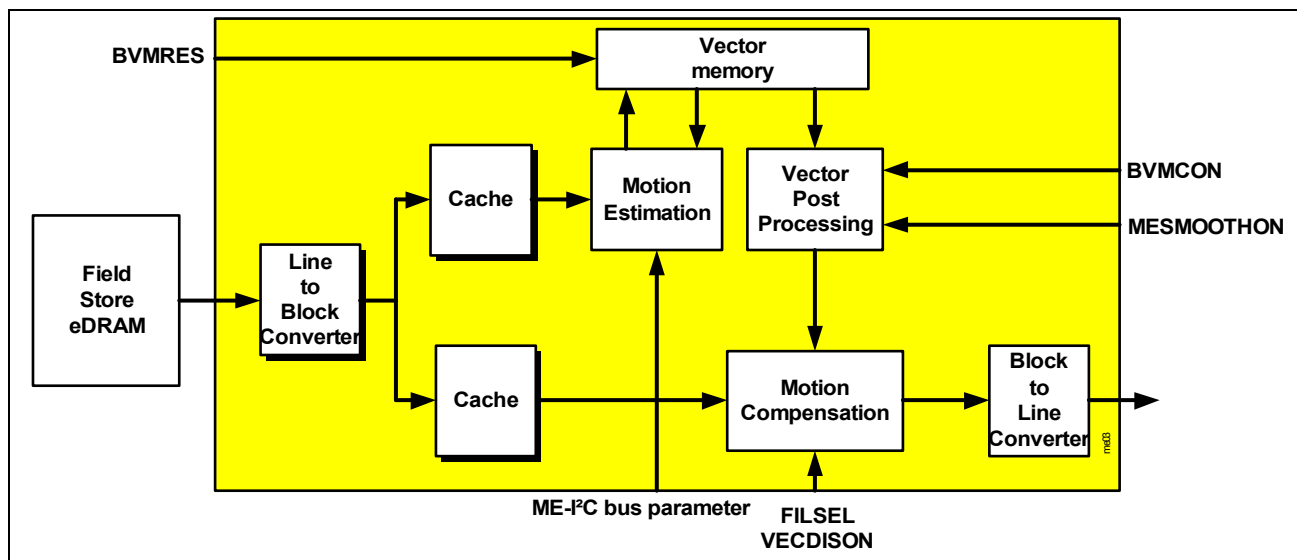


Figure 42 Block diagram of motion estimation and compensation

The **Figure 43** illustrates a more detailed block diagram of the motion estimation block. The motion estimation block is separated in two branches. The left one is only responsible for still area detection and the right one for all kind of areas. The additional left branch can be switched off or on by the I²C Bus parameter MENULLFUNON (I²C Bus parameter 4Bh). Different preprocessing blocks are located in both branches due to the different tasks of the branches. After preprocessing of the input data the main computation, the block matching, is executed.

For the right branch, the motion estimator applies two concurrent recursive block matchers, that individually check three candidate vectors with different convergence directions. Among the three candidates there is one spatial prediction vector taken from a previously processed block and a temporal prediction vector. The temporal prediction has the characteristic feature that its position is shifted with respect to the block currently processed in the opposite direction compared to the spatial prediction. The **Figure 44**

illustrates this feature, and shows that both types of predictions differ for the two estimators (Sa and Ta of the first estimator, Sb and Tb for the second). Both estimators further test one candidate that is found as the sum of their spatial prediction vector and an update vector. The last candidate is the null vector.

The left branch contains only a special null block matcher. The best matching null vector from either of the two branches is assigned to the current block.

The overall best vector is finally selected and used for scan rate conversion.

Different penalty mechanism exist to optimize the behaviour of the both branches of the motion estimation block.

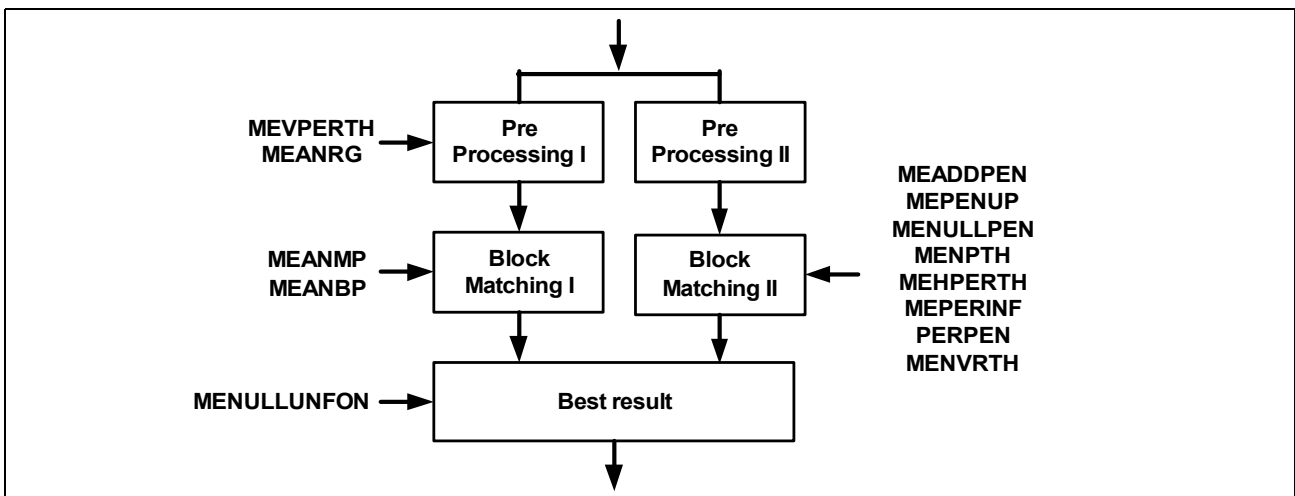


Figure 43 Block diagram of motion estimation

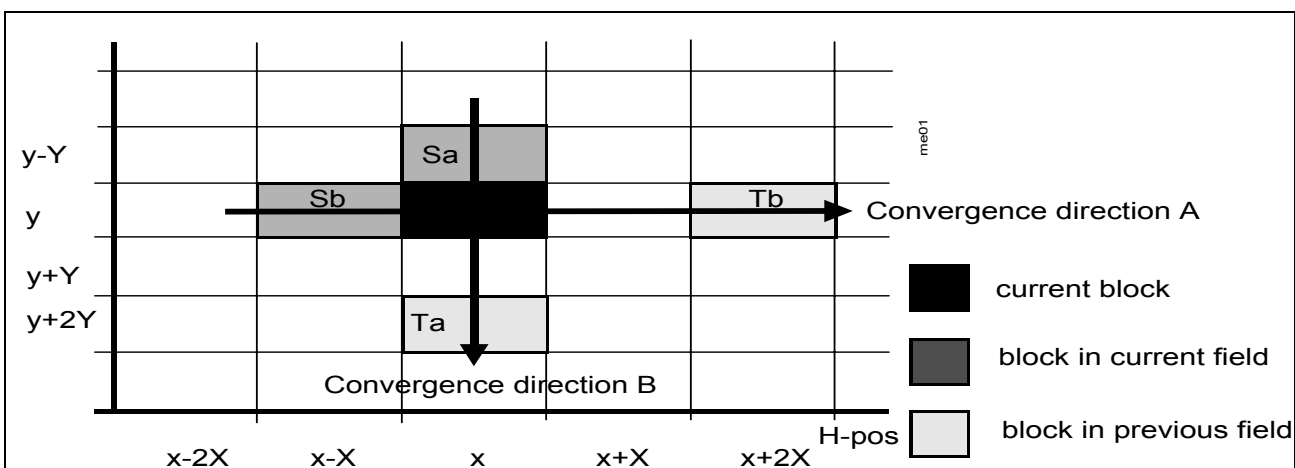


Figure 44 Relative positions of the spatial predictors

The I²C Bus parameters below are used for optimization purposes of the motion estimation block and should not be changed by the customer.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MEANBP | 50h | Penalty for border lines in additional null dbd (dbd - displaced block difference) |
| MEANMP | 50h | Penalty for middle lines in additional null dbd |
| MEANRG | 51h | Range of middle lines in additional null dbd |
| MEHPERTH | 51h | Threshold for horizontal periodicity detection |
| MEVPERTH | 51h | Threshold for vertical periodicity detection |
| MEPERINF | 50h | Defines influences of periodicity |
| BVMRES | 52h | Reset command for block vector memory - Channel switch (on switching to a new channel by remote control, switch on BVMRES once and release; note: reset film mode detection too [RESMOV]) - Freeze picture (on picture freeze switch on BVMRES and hold; alternative: switch to non motion compensated scan rate conversion [STOPMOM/ADOPMOM]) - SSC or MUP mode (on multipicture on double window/split screen display switch on BVMRES and hold) - Switch from SSC/MUP to SRC mode (switch to SRC mode, switch on BVMRES, change master channel display size to full screen [768x576], change back to normal master channel screen size and release BVMRES) - Vector memory reset takes place only on the active master channel output size; to reset the whole vector memory switch to maximum master channel size (768x576) - Minimum hold time for BVMRES to have an effect: on CAMERA MODE: 1 input field, on PAL FILM MODE: 2 input fields; on NTSC FILM MODE 3 input fields |
| PERPEN | 52h | Penalty for periodic structures |
| MENPTH | 50h | Minimum vector length for null dbd penalty |
| MENVRTH | 59h | Null vector reliability threshold, makes detection of null vector in homogenous areas more reliable. Threshold value to adjust sensibility of null vector reliability: 1111: insensible : 0001: sensible to motion and noise 0000: <u>off</u> |
| MENULLPEN | 4Fh | Additional penalty for null vector, if vector length exceeds length given by MENPTH and dbd of null vector is greater as a given threshold, which is defined by MENVRTH |
| MEPENUP | 4Ch | Penalty for update vectors |
| MEADDPEN | 4Ch | Additional penalty for non-null vectors |
| MESMOOTHON | 4Bh | Vector smoothing on/off |
| MENULLUNFON | 4Bh | Unfiltered null dbd on/off |
| BVMCON | 4Eh | Vector correction on/off |

Table 79 Output write I²C Bus parameter

5.9 Motion compensation

In the SDA 9415 the motion estimation algorithm is combined with an advanced scan rate conversion algorithm. The **Figure 45** shows the position of the fields as a function of the time for a 50 Hz sequence and a 100 Hz sequence. The information of the motion estimation (vector field) can be used for the generation of the additional fields. The A field is directly used as "a" field. The B field has the right position, but the wrong phase. The line-scanning pattern interpolation into a A field can be used as "c" field. The "b" and "d" field has to be generated using the vector field of the motion estimation.

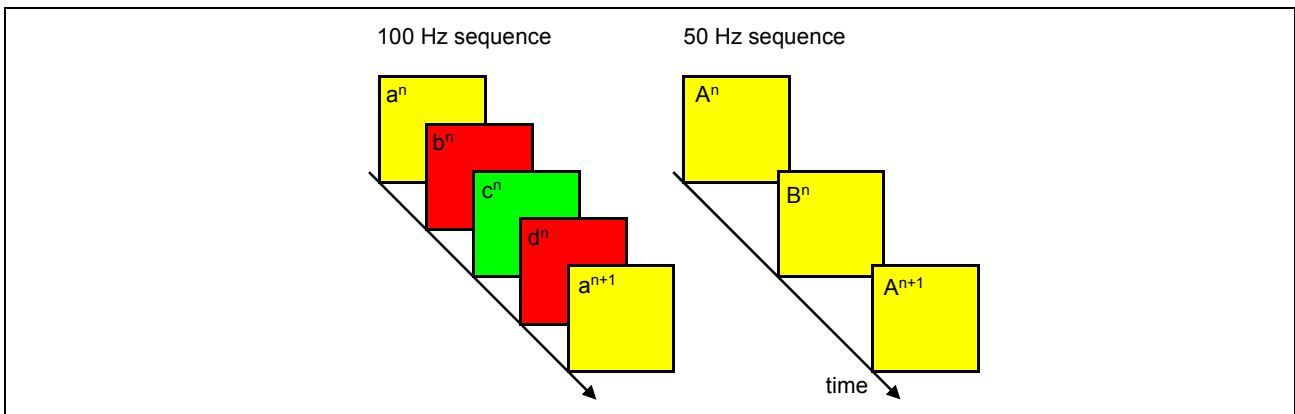


Figure 45 Timing of 100 Hz scan rate conversion

The **Figure 46** shows a moving object as a function of the time. The position of the object in the b field is exactly half the position of the object in the A and B field. That's why no double contours are visible.

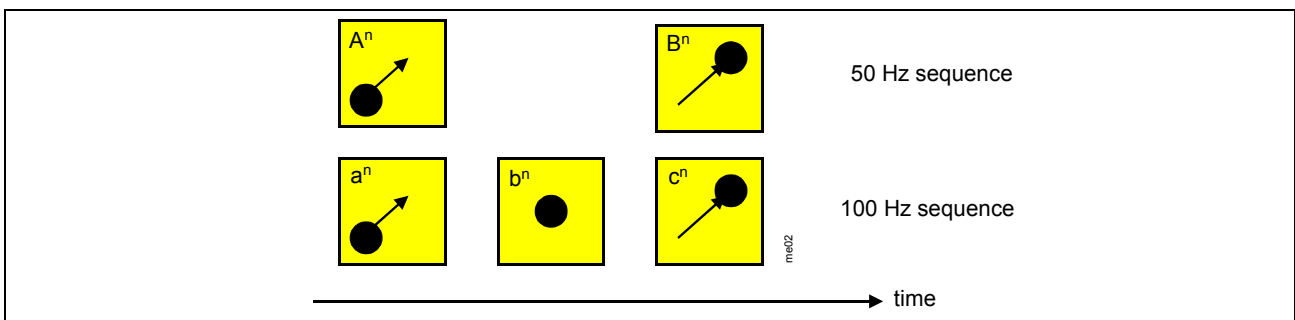


Figure 46 Principles of motion compensation

The principle of the up conversion process is illustrated in the **Figure 47** in case of the b field. Motion compensated pixels are fed to a 5-tap median filter. The background is that in case of correct motion vector, it can be expected that the two motion compensated pixels from both neighboring fields are identical. Consequently, either of the two is selected and a correctly motion compensated intermediate field results. In the figure below the vector ends on a non existing line. Therefore the pixels of the line before and after the non existing line are taken. Is the vector unreliable for the current pixel, the two

motion compensated pixels will be different, and the chance that the non-motion compensated field average at the output increases. The result is a graceful degradation of picture material in case of vector failure (“local fall back mode”).

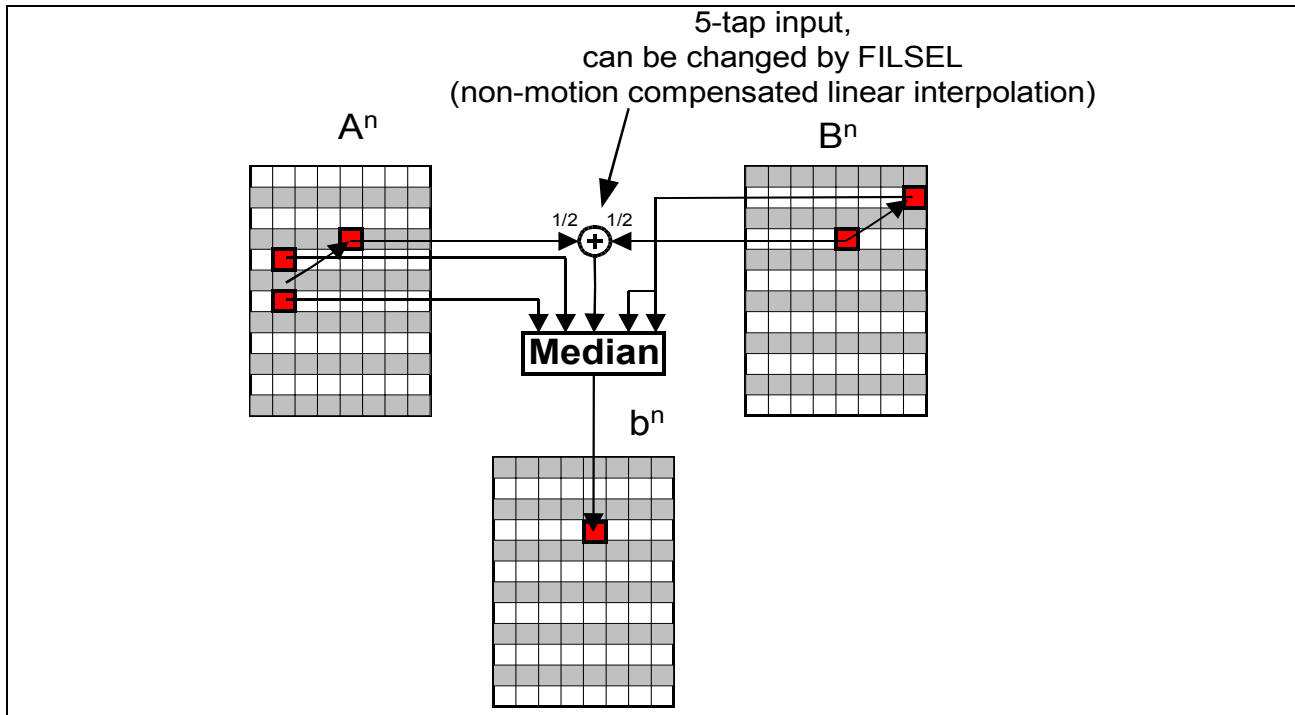


Figure 47 Principles of motion compensation for the β field (FILSEL=0)

To generate an output sequence with a good motion portrayal the estimated vectors and the actual film mode information are used. Dependent on the film mode different output sequences are generated. The standard mode is camera mode. In this mode the input source provides a new motion phase on every field. The two other modes are called film mode PAL and NTSC, respectively. They arise from scanning cinematic source material for which only 24 frames per second are available. For film mode material scanned for 50 Hz standards always two successive fields have the same motion phase. The film source is reproduced with 25 Hz and each image is scanned twice to get an interlaced video signal. On NTSC film mode the 24 frames are scanned using the 2-3 pulldown method resulting in sequences, which contain alternating two and three successive fields with the same motion phase. In the next figures the three modes are illustrated for a one-dimensional motion.

The aim on motion compensation is to create an output field or frame sequence, which has a good motion portrayal. In the **Figure 48**, **Figure 49** and **Figure 50** the ideal motion portrayal is displayed as a dashed line. The output motion (solid line) should approach this ideal case. The deviation is marked as shadowed area. On camera mode no motion blurring occurs on source material (**Figure 48**: square curve). A simple non motion compensated scan rate conversion repeats previous motion phases and causes a motion blurring on 100/120 Hz output dependent on motion speed (**Figure 48**: triangle

curve). With motion compensation (**Figure 48**: rhomb curve) intermediate motion phases are calculated and the ideal curve is obtained, no motion blurring occurs.

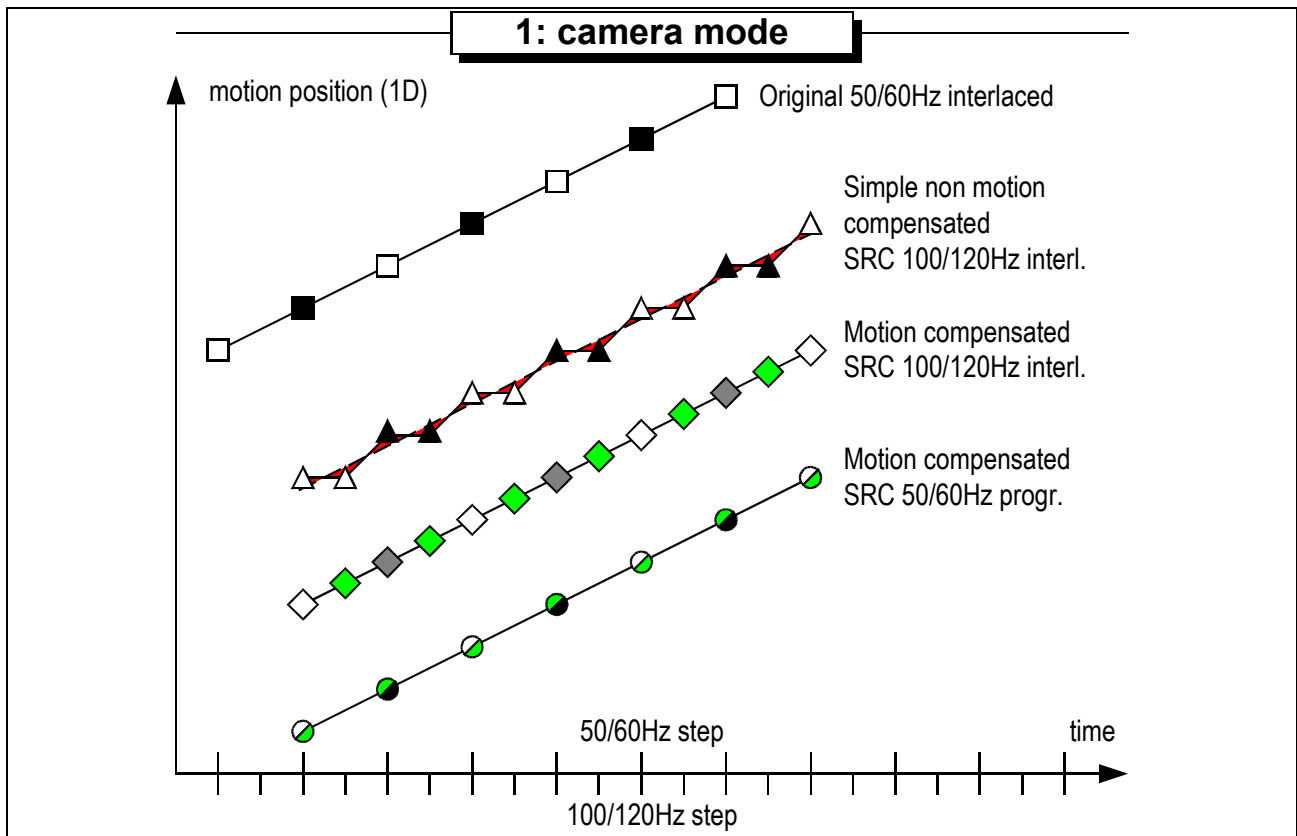


Figure 48 Output sequence generation: Camera mode

A 50 Hz film mode input sequence already shows a motion blur (**Figure 49**: square curve). This artifact increases on higher velocities. Motion compensation techniques can reduce this effect under a visible threshold. Now the deviation from the ideal curve is minimized (**Figure 49**; rhomb curve). The result is an output motion portrayal, which is visibly smoother compared with the original input sequence.

A 60 Hz input field sequence has motion artifacts on higher velocities (**Figure 50**: square curve) like the 50 Hz film mode but the blur is much more irregular caused by the 2-3 pulldown. The preferred application in this case is a 60 Hz progressive conversion. Here also the motion portrayal can be improved by creating a new motion phases (**Figure 50**: circle curve). Also this conversion results in a clearly improved motion portrayal.

Evaluation shows a very large improvement of the Film motion portrayal.

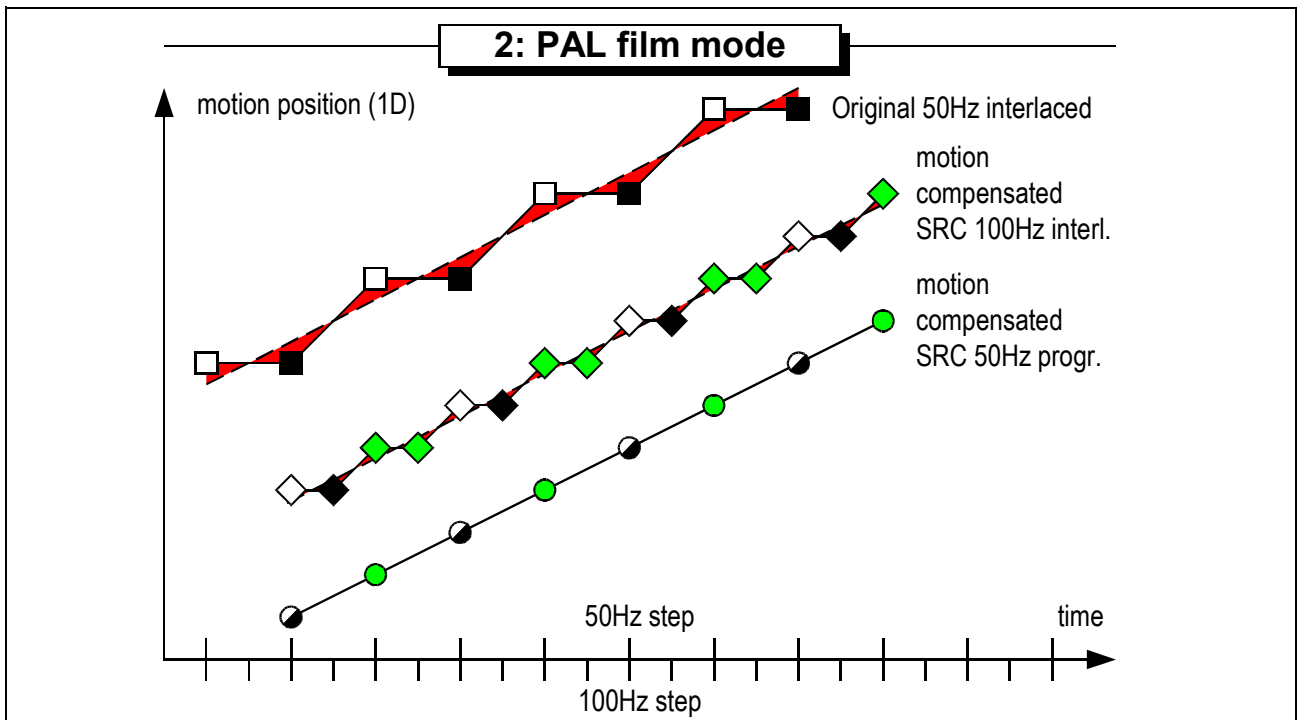


Figure 49 Output sequence generation: PAL film mode

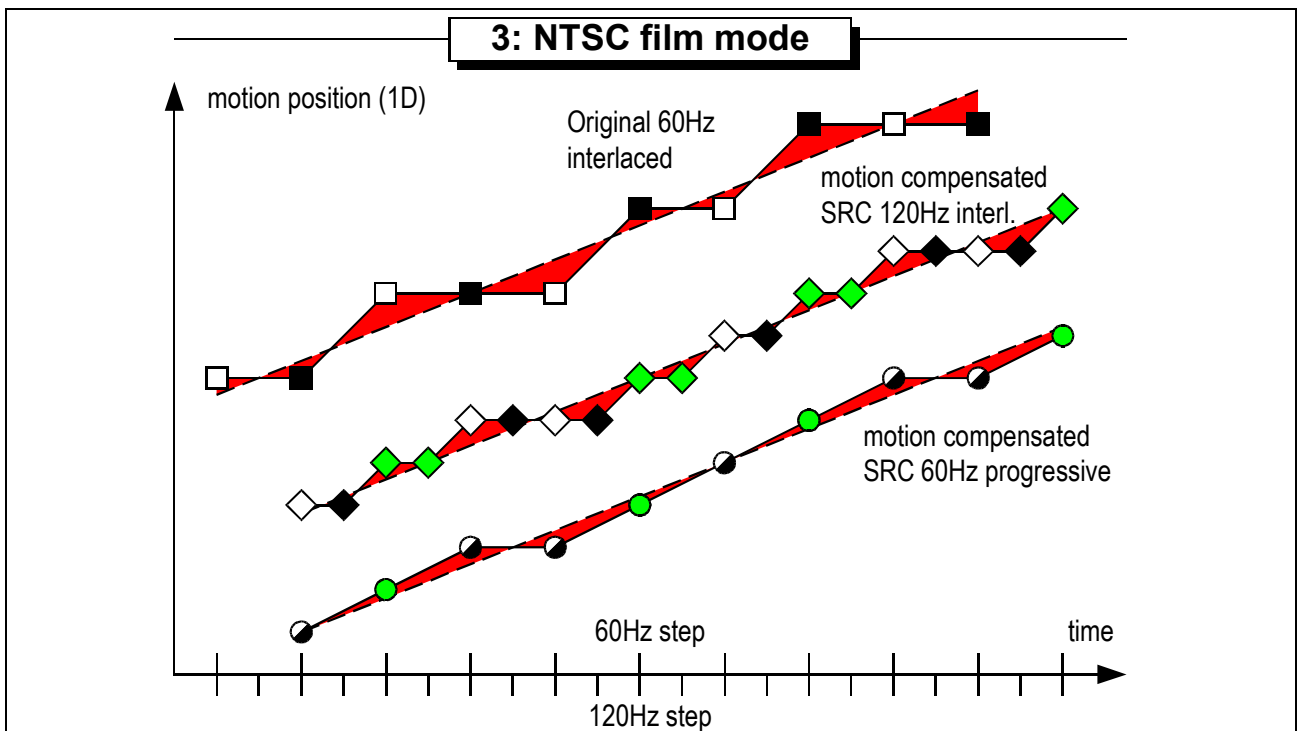












Figure 50 Output sequence generation: NTSC film mode

| | | | |
|-----------------------------------------------------------------------------------|------------------------------|-----------------------------------------------------------------------------------|----------------------------------------------------|
|  | Original A field information |  | 50/60Hz interlaced input |
|  | Original B field information |  | 100/120Hz non motion compensated interlaced output |
|  | Motion compensated field |  | 100/120Hz motion compensated interlaced output |
|  | Real motion course |  | 50/60Hz motion compensated progressive output |
|  | Ideal motion course |  | Deviation between real ideal motion course |

The scan rate conversion of the colour difference signals is also vector based. As it was experimentally found that the dynamic resolution of the colour is not masked completely by the luminance, motion compensated chrominance processing is implemented. The chrominance motion compensation uses the vector results of the luminance motion estimation.

The characteristic of the median filter can be changed by the I²C Bus parameter FILSEL.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FILSEL | 4B | Filter select for VDU interpolation 11: Improved median based interfield interpolation: for use in SRC mode and for use with frame based upconversion or field based upconversion with two field memories (STOPMOM 0000, 0001, 0010, 1011, 1100, 1110, 1111 for RMODE 0 or 1) 10: median based interfield interpolation: [not recommended] 01: linear INTRAFIELD interpolation: interpolation $(a_0+a_1)/2$ or $(b_0+b_1)/2$ for use in SSC and MUP mode or for use with field based scan rate conversion and only one field memory (STOPMOM 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100 for RMODE 0 or 1) 00: linear INTERFIELD interpolation: $(a_0+a_1+b_0+b_1)/4$ [not recommended] |

Table 80 Output write I²C Bus parameter

5.10 Global motion, film mode and phase detection

For camera mode and film mode different scan rate conversion algorithms and motion estimation processes are valid. Therefore the information about camera mode or film mode and the corresponding phase are necessary to adapt the processing. In the SDA 9415 the film mode, film type and phase detection is based on the analysis of the motion

vectors from the estimator or the analysis of the field difference. It is expected that with film material broadcast in the 50 Hz television standard, motion will occur only every second field. Therefore the “vector activity” (VAC) in the SDA 9415 as sum of the absolute vector components which are larger as a threshold defined by the I²C parameter MEMMINMOT (I²C Bus sub address 4Bh) is accumulated . Depending on the sum, the actual detected mode (MOVMO, MOV TYP) and several I²C Bus parameters (MEMINTH, MEMAXTH, SFMINTH, SFMAXTH) the actual field is decided to have motion or not. The table below explains the decision of the detection:

| Actual field has | If |
|------------------|-------------------------------------------------------------------------------------------------------------------|
| motion | [VAC > scmax * (MEMAXTH+1)] or [(VAC > scmin * (MEMINTH+1)) and (VAC <= scmax * (MEMAXTH+1)) and MOVMO=0] |
| no motion | [VAC <= scmin * (MEMINTH+1)] or [(VAC > scmin * (MEMINTH+1)) and (VAC <= scmax * (MEMAXTH+1)) and MOVMO=1] |

Table 81 Principles of global motion and film mode detection

The values scmin and scmax are scale factors which are defined by the table below:

| SFMINTH/SFMAXTH | scmin/scmax |
|-----------------|-------------|
| 00 | 8 |
| 01 | 16 |
| 10 | 32 |
| 11 | 64 |

Table 82 Definition of scmin/scmax depending on SFMINTH/SFMAXTH

To avoid switching artifacts a temporal hysteresis is implemented. Temporal hysteresis means, that at least a certain number of fields defined by the I²C Bus parameter MEMOHIST must fulfill the conditions for switching from camera mode to film mode or vice versa. The number of fields (NoFields) defined by the I²C Bus parameter MEMOHIST can be calculated by the equation below:

$$\text{NoFields} = 2 \bullet (\text{MEMOHIST} + 1)$$

Furthermore a global motion flag GMOTION is derived and the value MEMSTAT, which is proportional to the amount of blocks, which fulfill the condition mentioned above.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MOVPHIN 1: enabled 0: disabled | 4Bh | Inversion of the Film phase signal |
| MEMMINMOT | 4Bh | Minimum vector threshold for film mode and global motion detection |
| MEMINTH | 4Dh | Threshold for detection of motion in camera mode |
| MEMAXTH | 4Eh | Threshold for detection of motion in film mode |
| MEMOHIST | 4Fh | History length of Film mode and global motion detection |
| SFMINTH | 4Dh | Scale factor for MEMINTH |
| SFMAXTH | 4Dh | Scale factor for MEMAXTH |
| MEMMNDTH | 59h | Threshold for switching between the vector activity or the field difference as input for the film mode detection Use field difference as film mode detection input 1111: insensible to motion : 0001: sensible to motion 0000: use vector activity as film mode detection input |

Table 83 Output write I²C Bus parameter

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MOVMO | 7Eh | 1: Film mode 0: camera mode |
| MOVPH | 7Eh | Film mode phase: 1: B ⁿ and A ⁿ⁺¹ has the same phase 0: A ⁿ and B ⁿ has the same phase |
| GMOTION | 7Eh | Global motion detection 1: if no STILL scene is detected (minimum is: 1 field in motion of 32 fields in order) 0: if STILL scene is detected (32 fields in order without motion) |
| MOVTYP | 7Eh | Film mode type 1: NTSC film mode source with 24 motion phases per second (2-3 pull down) 0: PAL film mode source with 25 motion phases per second |
| MEMSTAT | 7Eh | Statistic about motion blocks |

Table 84 Output read I²C Bus parameter

5.11 Vertical expansion

For every output field, the scan rate converter generates a progressive frame. Thus for every output field period, a progressively scanned frame compensated to the correct motion is used for vertical expansion in case of Micronas VDU. This yields a highly improved performance compared with an intra-field zoom.

The table below defines the internal expansion factor ZOOM depending on the RMODE and VERINT I²C Bus parameter.

| VERINT | RMODE | ZOOM |
|--------------------------------|-------|--------------|
| I ² C Bus parameter | 0 | 2*(VERINT+1) |
| I ² C Bus parameter | 1 | (VERINT+1) |

Table 85 Output write I²C Bus parameter VERINT

The available expansion factors are listed in the table below.

| | 100/120 Hz interlaced RMODE=0 | 50/60 Hz progressive RMODE=1 | real vertical expansion factor |
|--------|----------------------------------|---------------------------------|-----------------------------------|
| VERINT | ZOOM | ZOOM | |
| 127 | 256 | 128 | 1.00 |
| : | : | : | : |
| 95 | 192 | 96 | 1.33 |
| : | : | : | : |
| 84 | 170 | 85 | 1.50 |
| : | : | : | : |
| 63 | 128 | 64 | 2.00 |

Table 86 Examples of reachable expansion factors

The I²C Bus parameter VPAN can be used to select the start line of the expansion. To expand the upper part of the incoming signal with the factor 2.0, VPAN should be set to zero. To expand the lower part, VPAN should be equal to 143. That means in case of VPAN=0 the first used line is line 1 and in case of VPAN=143 the first used line is line 144.

Dependent on the I²C Bus parameter VERINT a certain number of input lines of the input field is required. Therefore not all VPAN values are allowed. The formula below can be used to calculate the maximum allowed VPAN value depending on the chosen VERINT value.

$$VPAN_{max} = \left\lfloor 4 \cdot VERWIDTHM \cdot \left(1 - \frac{(VERINT + 1)}{128} \right) \right\rfloor$$

Floor symbol means: take only integer part of x

$$\lfloor x \rfloor$$

Figure 51 Calculation of maximum VPAN value

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|--------------------------------------------------------------|
| VERINT | 47h | Vertical expansion factor for master channel |
| VPAN | 54h | Vertical adjustment of the output picture for master channel |

Table 87 Output write I²C Bus parameter

5.12 Display processing

| Signals | Pin number | Description |
|---------|------------|--------------------------------------|
| IY_O | 87 | Analog Y (luminance) output signal |
| IU_O | 84 | Analog U (chrominance) output signal |
| IV_O | 90 | Analog V (chrominance) output signal |

Table 88 Output signals

The display processing part contains an integrated triple 9-bit DAC and performs digital enhancements and manipulations of the digital video component signal. The figure below shows the block diagram of the display processing part and the existing I²C Bus parameters.

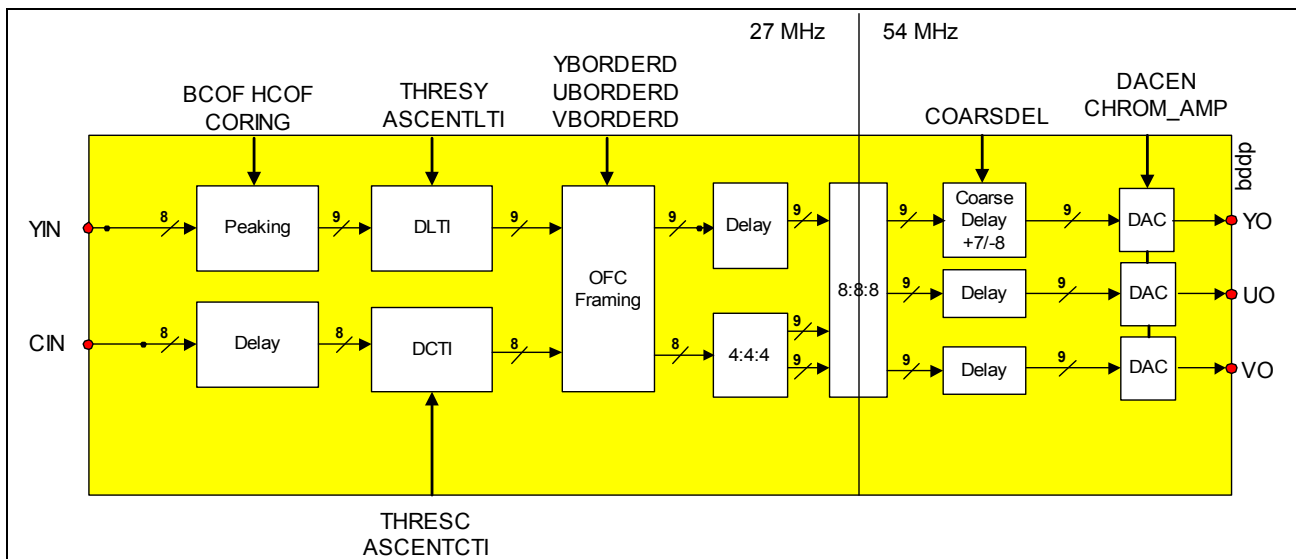


Figure 52 Block diagram of display processing

5.12.1 Peaking

The luminance peaking filter improves the over all frequency response of the luminance channel. It consists of two filters working in parallel. They have high pass (HP) and band pass (BP) characteristics. Their gain factors are separately programmable (I²C Bus parameters BCOF 5Dh, HCOF 5Dh). The high pass and the band pass filters are equipped with a common coring algorithm. It is optimized to achieve a smooth display of grey scales, not to improve the signal-to-noise ratio. Therefore no artifacts are produced. Coring can be switched off (I²C Bus parameter CORING, 5Ah). The figure below shows the block diagram of the peaking block.

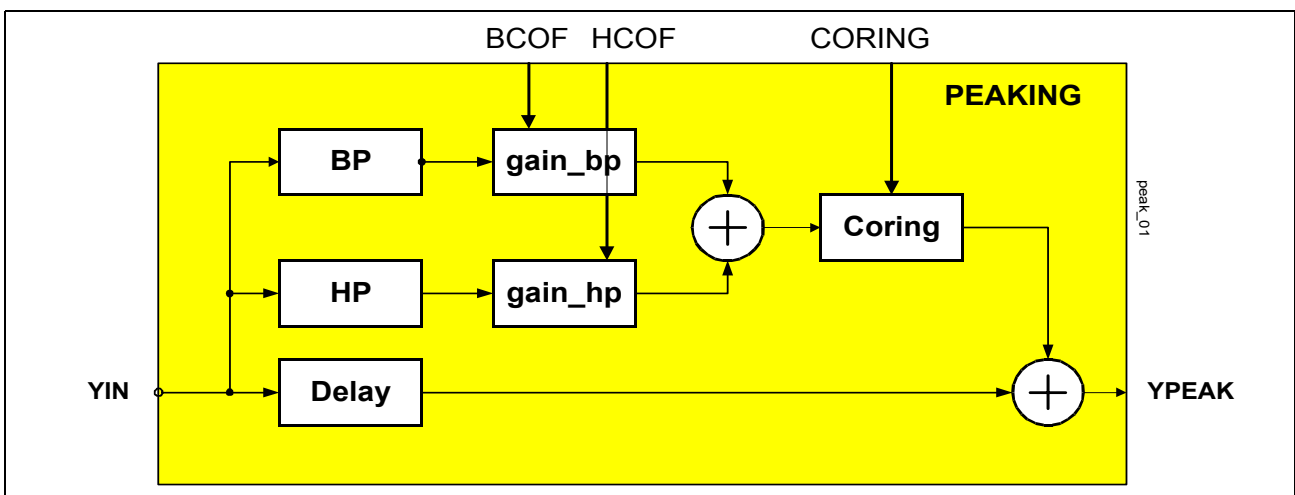


Figure 53 Block diagram peaking

The transfer functions of the separate filters are listed below:

High pass Transfer function: $HHP(z) = 1/16 (1-z^{-1})^4$

Band pass Transfer function: $HBP(z) = - 1/8 (1-z^{-2})^2$

All pass Transfer function: $HAP(z) = z^{-2}$

| BCOF | gain_bp | HCOF | gain_hp |
|------|---------|------|---------|
| 0 | 0 | 0 | 0 |
| 1 | 0.25 | 1 | 0.25 |
| 2 | 0.5 | 2 | 0.5 |
| 3 | 0.75 | 3 | 0.75 |
| 4 | 1 | 4 | 1 |
| 5 | 1.25 | 5 | 1.25 |
| 6 | 1.5 | 6 | 1.5 |
| 7 | 1.75 | 7 | 1.75 |
| 8 | 2 | 8 | 2 |
| 9 | 2.25 | 9 | 2.25 |
| 10 | 2.5 | 10 | 2.5 |
| 11 | 2.75 | 11 | 2.75 |
| 12 | 3 | 12 | 3 |
| 13 | 3.5 | 13 | 3.5 |
| 14 | 4 | 14 | 4 |
| 15 | 5 | 15 | 5 |

Table 89 Conversion table BCOF/HCOF to gain_bp/gain_hp

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|-----------------------------------------------------------|
| BCOF | 5Dh | Gain of band pass filter |
| HCOF | 5Dh | Gain of high pass filter |
| CORING | 5Ah | Coring for high- and band pass filter: 1: on 0: off |

Table 90 Output write I²C Bus parameters

5.12.2 Digital luminance transition improvement

A new digital algorithm is implemented to improve horizontal transitions of the luminance signals resulting in a better picture sharpness. A correction signal proportional to the slope of the detected horizontal transition of the input signal is added to the original input

signal. The amplitude of the correction signal is adjustable by the I²C Bus parameter ASCENTLTI.

The exact position of a luminance transition is calculated by detecting the corresponding zero transition of the second derivative of the luminance signal. Low pass filtering is performed to avoid noise sensitivity. The I²C Bus parameter THRESY and THRESY_UP defines the sensitivity of the DLTl circuit. High values cause that only significant luminance transitions are improved. Small luminance variations remain unchanged.

| THRESY | Sensitivity |
|--------|-------------|
| 000 | DLTI off |
| 001 | 4 |
| 010 | 8 |
| 011 | 12 |
| 100 | 16 |
| 101 | 20 |
| 110 | 24 |
| 111 | 28 |

Table 91 I²C Bus parameter THRESY

| THRESHY_UP | Amplitude |
|------------|-----------|
| 00 | off |
| 01 | 32 |
| 10 | 128 |
| 11 | 64 |

Table 92 I²C Bus parameter THRESY_UP

| ASCENTLTI | Amplitude |
|-----------|-----------|
| 00 | 0.5 |
| 01 | 1 |
| 10 | 2 |
| 11 | 4 |

Table 93 I²C Bus parameter ASCENTLTI

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|---------------------------------------------|
| THRESY | 5Eh | Defines lower sensitivity threshold of DLTl |
| THRESY_UP | 5Eh | Defines upper sensitivity threshold of DLTl |
| ASCENTLTI | 5Ch | Defines amplitude of correction signal |

Table 94 Output write I²C Bus parameters

5.12.3 Digital colour transition improvement

A new digital algorithm is implemented to improve horizontal transitions of the chrominance signals resulting in a better picture sharpness. A correction signal proportional to the slope of the detected horizontal transition of the input signal is added to the original input signal. Different correction signals according to the bandwidth of the input signal are selected. The amplitude of the correction signal is adjustable by the I²C Bus parameter ASCENTCTI.

The exact position of a colour transition is calculated by detecting the corresponding zero transition of the second derivative of both chrominance signals. Low pass filtering is performed to avoid noise sensitivity. The I²C Bus parameter THRESC modifies the sensitivity of the DCTI circuit. High values cause that only significant colour transitions are improved. Small colour variations remain unchanged.

To eliminate “wrong colours” transitions, which are caused by over and undershoots at the chroma transition, the sharpened chroma signals are limited to a proper value automatically.

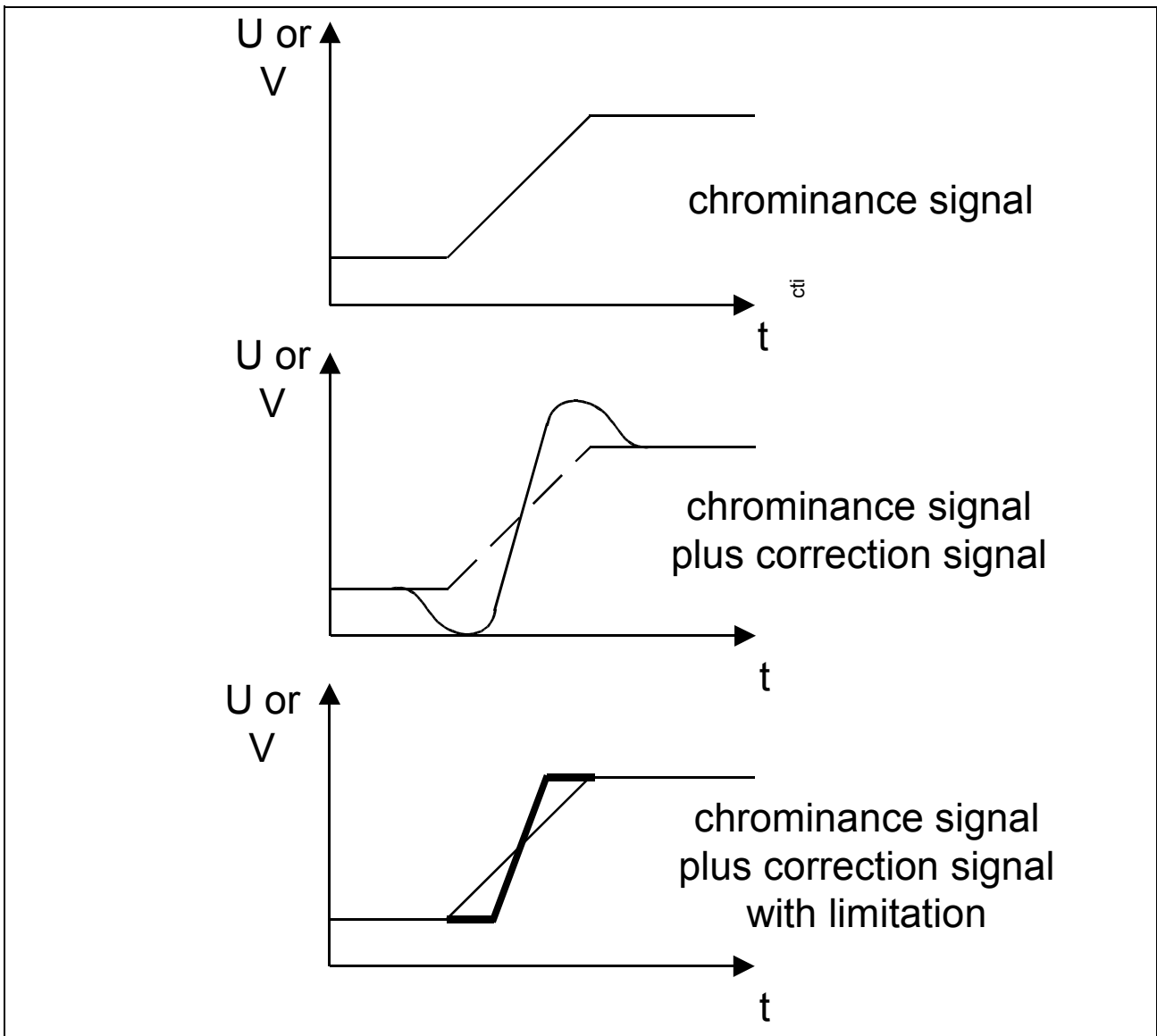


Figure 54 Principles of DCTI

| THRESC | Sensitivity |
|--------|-------------|
| 00 | DCTI off |
| 01 | 4 |
| 10 | 8 |
| 11 | 12 |

Table 95 I²C Bus parameter THRESC

| ASCENTCTI | Amplitude |
|-----------|-----------|
| 00 | 0.5 |
| 01 | 1 |
| 10 | 2 |
| 11 | 4 |

Table 96 I²C Bus parameter ASCENTCTI

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|----------------------------------------|
| THRESC | 5Eh | Defines sensitivity of DCTI |
| ASCENTCTI | 5Ch | Defines amplitude of correction signal |

Table 97 Output write I²C Bus parameters

5.12.4 Output format conversion

The SDA 9415 supports at the output side (digital output) the sample frequency relations of Y : (B-Y) : (R-Y): 4:2:2. The representation of the samples of the chrominance signal is programmable as positive dual code (unsigned, parameter TWOOUT=0) or two's complement code (TWOOUT=1, see "I²C Bus" on page 123, I²C bus parameter 5Ah).

| Data Pin | 4:2:2 Parallel | |
|----------|-----------------|-----------------|
| YOUT7 | Y ₀₇ | Y ₁₇ |
| YOUT6 | Y ₀₆ | Y ₁₆ |
| YOUT5 | Y ₀₅ | Y ₁₅ |
| YOUT4 | Y ₀₄ | Y ₁₄ |
| YOUT3 | Y ₀₃ | Y ₁₃ |
| YOUT2 | Y ₀₂ | Y ₁₂ |
| YOUT1 | Y ₀₁ | Y ₁₁ |
| YOUT0 | Y ₀₀ | Y ₁₀ |
| UVOUT7 | U ₀₇ | V ₀₇ |
| UVOUT6 | U ₀₆ | V ₀₆ |
| UVOUT5 | U ₀₅ | V ₀₅ |
| UVOUT4 | U ₀₄ | V ₀₄ |
| UVOUT3 | U ₀₃ | V ₀₃ |
| UVOUT2 | U ₀₂ | V ₀₂ |
| UVOUT1 | U ₀₁ | V ₀₁ |
| UVOUT0 | U ₀₀ | V ₀₀ |

Table 98 Output write parameters

X ab: X: signal component a: sample number b: bit number

The digital output and the analog output can not be used together. Either the digital output or the analog output can be enabled. Therefore in the SDA 9415 a circuit is implemented, which allows only enabling of the digital or analog outputs.

| Parameter | Subaddress | Description |
|-------------------------------------|------------|-----------------------------------------|
| DACEN 1: Enabled 0: Disabled | 5Ah | Enables the Digital-to-Analog converter |
| DOUTEN 1: Enabled 0: Disabled | 5A | Enables the digital output pins |

Table 99 Output write parameters

5.12.5 Insertion facilities

Two different values are inserted into the video signal: black level and coloured background area. The black level insertion is done automatically in the SDA 9415. The black level is inserted in the horizontal and vertical blanking period.

The second insertion facility produces a coloured background area on the display controlled by the I²C Bus parameters YBORDERD, UBORDERD and VBORDERD.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| YBORDERD | 5Ah | Y border value of display (Yborderd(3) Yborderd(2) Yborderd(1) Yborderd(0) 0 0 0 0 = 00010000 = 16), YBORDERD defines the 4 MSB's of a 8 bit value |
| UBORDERD | 5Bh | U border value of display (Uborderd(3) Uborderd(2) Uborderd(1) Uborderd(0) 0 0 0 0 = 10000000 = 128), UBORDERD defines the 4 MSB's of a 8 bit value |
| VBORDERD | 5Bh | V border value of display (Vborderd(3) Vborderd(2) Vborderd(1) Vborderd(0) 0 0 0 0 = 10000000 = 128), VBORDERD defines the 4 MSB's of a 8 bit value |

Table 100 Output write I²C Bus parameters

5.12.6 Coarse delay

Before Digital-to-Analog conversion an adjustment of the phase of the luminance signal can be performed (I²C Bus parameter COARSDEL, 5Ch). The delay of the luminance can be varied by periods (-8, ...[1]... , +7) of the DAC clock (2*CLKD). This can be used to compensate different delay times of external analog filters.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|--------------------------------------------------------------------------------------|
| COARSDEL | 5Ch | Delay of the luminance signal in relation to the chrominance signal in 2*CLKD clocks |

Table 101 Output write I²C Bus parameter

5.12.7 Digital-to-Analog conversion

Three 9-bit Digital-to-Analog converters are implemented. The DACs are short-circuit protected converters with current outputs. The full range output current of the IY_O, IU_O, IV_O channels (I_{OFR}) is determined by the current I_{REF} at the pin RREF_I by $I_{OFR} \sim 10 I_{REF}$. The voltage at the pin RREF_I is generated via pin UREF_I by an internal operational amplifier and follows the voltage at the pin UREF_I. Thus I_{REF} is given by $I_{REF} \sim V_{UREF}/R_{REF}$ where R_{REF} is a resistor between RREF_I and analog ground. Another way to define I_{REF} is the application of a current sink at the RREF_I point. For recommended values of V_{UREF} and I_{REF} compare "**Operating range**" on page 177. For applications with lower requirements there is still another way to define I_{OFR} : Connect pin UREF_I to the positive supply and apply a resistor against ground. Since in this operation mode the internal reference amplifier reaches saturation, the exact value of I_{REF} is not exactly predictable.

| I ² C Bus parameter | Sub address | Description |
|--------------------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------|
| CHROM_AMP | 5Eh | Chrominance amplification factor adjustment for DAC output 1: amplification factor 2 0: <u>amplification factor 1</u> |

Table 102 Output write I²C Bus parameter

5.13 I²C Bus

5.13.1 I²C Bus slave address

Write Address: BCh

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
|---|---|---|---|---|---|---|---|

Read Address: BDh

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|

5.13.2 I²C Bus format

The SDA 9415 I²C Bus interface acts as a slave receiver and a slave transmitter and provides two different access modes (write, read). All modes run with a sub address auto increment. The interface supports the normal 100 kHz transmission speed as well as the high speed 400 kHz transmission.

write:

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|-------------|---|-----------|---|-------|---|---|
| S | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | A | Sub address | A | Data Byte | A | ***** | A | P |
|---|---|---|---|---|---|---|---|---|---|-------------|---|-----------|---|-------|---|---|

S: Start condition

A: Acknowledge

P: Stop condition

NA: Not Acknowledge

read:

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|-------------|---|---|---|---|---|---|---|---|---|---|
| S | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | A | Sub address | A | S | 1 | 0 | 1 | 1 | 1 | 0 | 1 | A |
|---|---|---|---|---|---|---|---|---|---|-------------|---|---|---|---|---|---|---|---|---|---|

| | | | | |
|-----------|---|-----------|----|---|
| Data Byte | A | Data Byte | NA | P |
|-----------|---|-----------|----|---|

The transmitted data are internally stored in registers. The master has to write a don't care byte to the sub address FFh (store command) to make the register values available for the SDA 9415. To have a defined time step, where the data will be available, the data are made valid with the incoming V-sync VINM or VINS or with the next OPSTARTM pulse, which is an internal signal and indicates the start of a new output cycle. The sub addresses, where the data are made valid with the VINM signal are indicated in the overview of the sub addresses with „VIM“, where the data are made valid with the VINS are indicated with „VIS“ and where the data are made valid with the OPSTARTM are indicated with „OS“. The I²C parameter VIMSTATUS, VISSTATUS and OSSTATUS (sub address 80h, 81h, 82h) reflect the state of the register values. If these bits are read as

'1', then the store command was sent, but the data aren't made available yet. If these bits are '0' then the data were made valid and a new write or read cycle can start. The bits VIMSTATUS, VISSTATUS and OSSTATUS may be checked before writing or reading new data, otherwise data can be lost by overwriting.

Furthermore the bits NMSTATUS (status of noise measurement: NOISEME) and LBDSTATUS (status of letter box I²C Bus parameters: SLAA, ELAA, STATUS_SLAA, STATUS_ELAA, RELY) exist. NMSTATUS signalizes a new value for NOISEME. So if NMSTATUS is read as '0' the current noise measurement has not been updated. If the NMSTATUS is read as '1' a new noise measurement value can be read. LBSTATUS signalizes at least a change of one of the I²C Bus parameters: SLAA, ELAA, STATUS_SLAA, STATUS_ELAA, RELY. If the LBDSTATUS is read as '0' none of the I²C Bus parameters has changed its value. If the LBDSTATUS is read as '1' at least one of the I²C Bus parameters has changed its value.

The transmitted data are internally stored in registers. Writing or reading from a not existing register is permitted and does not generate a fault by the IC.

After switching on the IC (after reset), all bits of the SDA 9415 are set to defined states. Particularly :

| Sub address | Default value | R/W | Take over | Sub address | Default value | R/W | Take over |
|-------------|---------------|-----|-----------|-------------|---------------|-----|-----------|
| 00 | 00h | W | VIM | 37 | 48h | W | OS |
| 01 | 00h | W | VIM | 38 | 9Ch | W | OS |
| 02 | 00h | W | VIM | 39 | 00h | W | OS |
| 03 | 00h | W | VIM | 3A | 00h | W | OS |
| 04 | 61h | W | VIM | 3B | 00h | W | OS |
| 05 | 88h | W | VIM | 3C | 00h | W | OS |
| 06 | 00h | W | VIM | 3D | 00h | W | OS |
| 07 | 40h | W | VIM | 3E | 5Ah | W | OS |
| 08 | 00h | W | VIM | 3F | B4h | W | OS |
| 09 | 00h | W | VIM | 40 | 48h | W | OS |
| 0A | 00h | W | VIM | 41 | 90h | W | OS |
| 0B | 69h | W | VIM | 42 | 00h | W | OS |
| 0C | 00h | W | VIM | 43 | 5Ah | W | OS |
| 0D | 90h | W | VIM | 44 | B4h | W | OS |
| 0E | B4h | W | VIM | 45 | B0h | W | OS |
| 0F | B4h | W | VIM | 46 | 10h | W | OS |
| 10 | 90h | W | VIM | 47 | 7Fh | W | OS |
| 11 | 00h | W | VIM | 48 | 00h | W | OS |
| 12 | 50h | W | VIM | 49 | 00h | W | OS |

| Sub address | Default value | R/W | Take over | Sub address | Default value | R/W | Take over |
|-------------|---------------|-----|-----------|-------------|---------------|-----|-----------|
| 13 | not used | | | 4A | 00h | W | OS |
| 14 | 09h | W | VIM | 4B | 8Dh | W | OS |
| 15 | FFh | W | VIM | 4C | 88h | W | OS |
| 16 | 00h | W | VIM | 4D | 87h | W | OS |
| 17 | FFh | W | VIM | 4E | 3Fh | W | OS |
| 18 | 81h | W | VIM | 4F | 38h | W | OS |
| 19 | 01h | W | VIM | 50 | 56h | W | OS |
| 1A | 1Ch | W | VIM | 51 | 64h | W | OS |
| 1B | AAh | W | VIM | 52 | 3Ah | W | OS |
| 1C | 78h | W | VIM | 53 | 08h | W | OS |
| 1D | C6h | W | VIM | 54 | 00h | W | OS |
| 1E | 32h | W | VIM | 55 | 08h | W | OS |
| 1F | 57h | W | VIM | 56 | 78h | W | OS |
| 20 | 1Ch | W | VIM | 57 | 02h | W | OS |
| 21 | not used | | | 58 | 02h | W | OS |
| 22 | 00h | W | VIS | 59 | 00h | W | OS |
| 23 | 00h | W | VIS | 5A | 21h | W | OS |
| 24 | 00h | W | VIS | 5B | 88h | W | OS |
| 25 | 00h | W | VIS | 5C | 58h | W | OS |
| 26 | 61h | W | VIS | 5D | 44h | W | OS |
| 27 | 88h | W | VIS | 5E | 73h | W | OS |
| 28 | 00h | W | VIS | 5F | 20h | W | OS |
| 29 | 40h | W | VIS | 60-77 | not used | | |
| 2A | 00h | W | VIS | 78 | | R | |
| 2B | 00h | W | VIS | 79 | | R | |
| 2C | 00h | W | VIS | 7A | | R | |
| 2D | E9h | W | VIS | 7B | | R | |
| 2E | 00h | W | VIS | 7C | | R | |
| 2F | 90h | W | VIS | 7D | | R | |
| 30 | B4h | W | VIS | 7E | | R | |
| 31 | B4h | W | VIS | 7F | | R | |
| 32 | 90h | W | VIS | 80 | | R | |
| 33 | 00h | W | VIS | 81 | | R | |
| 34 | 28h | W | VIS | 82 | | R | |

| Sub address | Default value | R/W | Take over | Sub address | Default value | R/W | Take over |
|-------------|---------------|-----|-----------|-------------|---------------|-----|-----------|
| 35 | 00h | W | OS | 83-FE | not used | | |
| 36 | 16h | W | OS | FF | | W | |

R/W: R - Read register; W - Write Register; R/W - Read and Write Register;
 Take over: VIM - take over with VINM; VIS - take over with VINS; OS - take over with OPSTARTM

5.13.3 I²C Bus commands

| Subadd. (Hex.) | Data Byte | | | | | | | |
|-------------------|--------------------|--------------------|--------------------|-------------------|--------------------|--------------------|--------------------|--------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | x | x | x | PLLMOFF PLLM | PLLMRA3 PLLM | PLLMRA2 PLLM | PLLMRA1 PLLM | PLLMRA0 PLLM |
| 01 | IPOSYM7 VHCOM | IPOSYM6 VHCOM | IPOSYM5 VHCOM | IPOSYM4 VHCOM | IPOSYM3 VHCOM | IPOSYM2 VHCOM | IPOSYM1 VHCOM | IPOSYM0 VHCOM |
| 02 | IPOXM7 VHCOM | IPOXM6 VHCOM | IPOXM5 VHCOM | IPOXM4 VHCOM | IPOXM3 VHCOM | IPOXM2 VHCOM | IPOXM1 VHCOM | IPOXM0 VHCOM |
| 03 | LEBORDM2 VHCOM | LEBORDM1 VHCOM | LEBORDM0 VHCOM | RIBORDM2 VHCOM | RIBORDM1 VHCOM | RIBORDM0 VHCOM | CHFILM1 VHCOM | CHFILM0 VHCOM |
| 04 | DELM2 IFC | DELM1 IFC | DELM0 IFC | FORCOLM VHCOM | YBORDERM3 VHCOM | YBORDERM2 VHCOM | YBORDERM1 VHCOM | YBORDERM0 VHCOM |
| 05 | UBORDERM3 VHCOM | UBORDERM2 VHCOM | UBORDERM1 VHCOM | UBORDEM0 VHCOM | VBORDERM3 VHCOM | VBORDERM2 VHCOM | VBORDERM1 VHCOM | VBORDERM0 VHCOM |
| 06 | UPBORDM3 VHCOM | UPBORDM2 VHCOM | UPBORDM1 VHCOM | UPBORDM0 VHCOM | LWBORDM3 VHCOM | LWBORDM2 VHCOM | LWBORDM1 VHCOM | LWBORDM0 VHCOM |
| 07 | INTHM12 VHCOM | INTHM11 VHCOM | INTHM10 VHCOM | INTHM9 VHCOM | INTHM8 VHCOM | INTHM7 VHCOM | INTHM6 VHCOM | INTHM5 VHCOM |
| 08 | INTHM4 VHCOM | INTHM3 VHCOM | INTHM2 VHCOM | INTHM1 VHCOM | INTHM0 VHCOM | DEZHM2 VHCOM | DEZHM1 VHCOM | DEZHM0 VHCOM |
| 09 | INTVM8 VHCOM | INTVM7 VHCOM | INTVM6 VHCOM | INTVM5 VHCOM | INTVM4 VHCOM | INTVM3 VHCOM | INTVM2 VHCOM | INTVM1 VHCOM |

| | | | | | | | | |
|----|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------------------|-------------------|
| 0A | INTVM0 VHCOM | DEZVM2 VHCOM | DEZVM1 VHCOM | DEZVM0 VHCOM | YPEAKM1 VHCOM | YPEAKM0 VHCOM | CPEAKM1 VHCOM | CPEAKM0 VHCOM |
| 0B | x | FORMATM1 IFC | FORMATM0 IFC | FIENVM ISC | VCRMODEM ISC | NAPIPPHM1 ISC | NAPIPPHM0 ISC | TWOINM IFC |
| 0C | NAPIPDL7 ISC | NAPIPDL6 ISC | NAPIPDL5 ISC | NAPIPDL4 ISC | NAPIPDL3 ISC | NAPIPDL2 ISC | NAPIPDL1 ISC | NAPIPDL0 ISC |
| 0D | ALPFM7 ISC | ALPFM6 ISC | ALPFM5 ISC | ALPFM4 ISC | ALPFM3 ISC | ALPFM2 ISC | ALPFM1 ISC | ALPFM0 ISC |
| 0E | APPLM7 ISC | APPLM6 ISC | APPLM5 ISC | APPLM4 ISC | APPLM3 ISC | APPLM2 ISC | APPLM1 ISC | APPLM0 ISC |
| 0F | APPLIPM7 ISC | APPLIPM6 ISC | APPLIPM5 ISC | APPLIPM4 ISC | APPLIPM3 ISC | APPLIPM2 ISC | APPLIPM1 ISC | APPLIPM0 ISC |
| 10 | ALPFIPM7 ISC | ALPFIPM6 ISC | ALPFIPM5 ISC | ALPFIPM4 ISC | ALPFIPM3 ISC | ALPFIPM2 ISC | ALPFIPM1 ISC | ALPFIPM0 ISC |
| 11 | VINDELM5 ISC | VINDELM4 ISC | VINDELM3 ISC | VINDELM2 ISC | VINDELM1 ISC | VINDELM0 ISC | VINPOLM ISC | HINPOLM ISC |
| 12 | x | NALIPM4 ISC | NALIPM3 ISC | NALIPM2 ISC | NALIPM1 ISC | NALIPM0 ISC | CHRFORM1 VHCOM | CHRFORM0 VHCOM |
| 13 | x | x | x | x | x | x | x | x |
| 14 | x | x | NMLINE4 TSNR | NMLINE3 TSNR | NMLINE2 TSNR | NMLINE1 TSNR | NMLINE0 TSNR | NMALG TSNR |
| 15 | TNRCLY3 TSNR | TNRCLY2 TSNR | TNRCLY1 TSNR | TNRCLY0 TSNR | TNRCLC3 TSNR | TNRCLC2 TSNR | TNRCLC1 TSNR | TNRCLC0 TSNR |
| 16 | TNRKOY3 TSNR | TNRKOY2 TSNR | TNRKOY1 TSNR | TNRKOY0 TSNR | TNRKOC3 TSNR | TNRKOC2 TSNR | TNRKOC1 TSNR | TNRKOC0 TSNR |
| 17 | TNRVAY3 TSNR | TNRVAY2 TSNR | TNRVAY1 TSNR | TNRVAY0 TSNR | TNRVAC3 TSNR | TNRVAC2 TSNR | TNRVAC1 TSNR | TNRVAC0 TSNR |
| 18 | TNRSEL TSNR | TNRHOY5 TSNR | TNRHOY4 TSNR | TNRHOY3 TSNR | TNRHOY2 TSNR | TNRHOY1 TSNR | TNRHOY0 TSNR | TNRFIY TSNR |
| 19 | x | TNRHOC5 TSNR | TNRHOC4 TSNR | TNRHOC3 TSNR | TNRHOC2 TSNR | TNRHOC1 TSNR | TNRHOC0 TSNR | TNRFIC TSNR |
| 1A | SNRON TSNR | PANAON VHCOM | PANAST3 TSNR | PANAST2 TSNR | PANAST1 TSNR | PANAST0 TSNR | NRON TSNR | DTNRON TSNR |
| 1B | OPDELM7 ISC | OPDELM6 ISC | OPDELM5 ISC | OPDELM4 ISC | OPDELM3 ISC | OPDELM2 ISC | OPDELM1 ISC | OPDELM0 ISC |

| | | | | | | | | |
|----|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 1C | TH_DN_BN5 LBD | TH_DN_BN4 LBD | TH_DN_BN3 LBD | TH_DN_BN2 LBD | TH_DN_BN1 LBD | TH_DN_BN0 LBD | TH_LB5 LBD | TH_LB4 LBD |
| 1D | TH_LB3 LBD | TH_LB2 LBD | TH_LB1 LBD | TH_LB0 LBD | TH_ALB3 LBD | TH_ALB2 LBD | TH_ALB1 LBD | TH_ALB0 LBD |
| 1E | x | TH_AA6 LBD | TH_AA5 LBD | TH_AA4 LBD | TH_AA3 LBD | TH_AA2 LBD | TH_AA1 LBD | TH_AA0 LBD |
| 1F | TH_MUNSL3 LBD | TH_MUNSL2 LBD | TH_MUNSL1 LBD | TH_MUNSL0 LBD | TH_AUNS3 LBD | TH_AUNS2 LBD | TH_AUNS1 LBD | TH_AUNS0 LBD |
| 20 | x | x | x | TH_MA_AA3 LBD | TH_MA_AA2 LBD | TH_MA_AA1 LBD | TH_MA_AA0 LBD | VOLBD LBD |
| 21 | x | x | x | x | x | x | x | x |
| 22 | x | x | x | PLLSOFF PLLS | PLLSRA3 PLLS | PLLSRA2 PLLS | PLLSRA1 PLLS | PLLSRA0 PLLS |
| 23 | IPOSYS7 VHCOM | IPOSYS6 VHCOM | IPOSYS5 VHCOM | IPOSYS4 VHCOM | IPOSYS3 VHCOM | IPOSYS2 VHCOM | IPOSYS1 VHCOM | IPOSYS0 VHCOM |
| 24 | IPOSXS7 VHCOM | IPOSXS6 VHCOM | IPOSXS5 VHCOM | IPOSXS4 VHCOM | IPOSXS3 VHCOM | IPOSXS2 VHCOM | IPOSXS1 VHCOM | IPOSXS0 VHCOM |
| 25 | LEBORDS2 VHCOM | LEBORDS1 VHCOM | LEBORDS0 VHCOM | RIBORDS2 VHCOM | RIBORDS1 VHCOM | RIBORDS0 VHCOM | CHFILS1 VHCOM | CHFILS0 VHCOM |
| 26 | DELS2 IFC | DELS1 IFC | DELS0 IFC | FORCOLS VHCOM | YBORDERS3 VHCOM | YBORDERS2 VHCOM | YBORDERS1 VHCOM | YBORDERS0 VHCOM |
| 27 | UBORDERS3 VHCOM | UBORDERS2 VHCOM | UBORDERS1 VHCOM | UBORDERS0 VHCOM | VBORDERS3 VHCOM | VBORDERS2 VHCOM | VBORDERS1 VHCOM | VBORDERS0 VHCOM |
| 28 | UPBORDS3 VHCOM | UPBORDS2 VHCOM | UPBORDS1 VHCOM | UPBORDS0 VHCOM | LWBORDS3 VHCOM | LWBORDS2 VHCOM | LWBORDS1 VHCOM | LWBORDS0 VHCOM |
| 29 | INTHS12 VHCOM | INTHS11 VHCOM | INTHS10 VHCOM | INTHS9 VHCOM | INTHS8 VHCOM | INTHS7 VHCOM | INTHS6 VHCOM | INTHS5 VHCOM |
| 2A | INTHS4 VHCOM | INTHS3 VHCOM | INTHS2 VHCOM | INTHS1 VHCOM | INTHS0 VHCOM | DEZHS2 VHCOM | DEZHS1 VHCOM | DEZHS0 VHCOM |
| 2B | INTVS8 VHCOM | INTVS7 VHCOM | INTVS6 VHCOM | INTVS5 VHCOM | INTVS4 VHCOM | INTVS3 VHCOM | INTVS2 VHCOM | INTVS1 VHCOM |
| 2C | INTVS0 VHCOM | DEZVS2 VHCOM | DEZVS1 VHCOM | DEZVS0 VHCOM | YPEAKS1 VHCOM | YPEAKS0 VHCOM | CPEAKS1 VHCOM | CPEAKS0 VHCOM |
| 2D | SLAVECON IFC | FORMATS1 IFC | FORMATS0 IFC | FIEINVS ISC | VCRModes ISC | NAPIPPHS1 ISC | NAPIPPHS0 ISC | TWOINS IFC |

| | | | | | | | | |
|----|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 2E | NAPIPDL7 ISC | NAPIPDL6 ISC | NAPIPDL5 ISC | NAPIPDL4 ISC | NAPIPDL3 ISC | NAPIPDL2 ISC | NAPIPDL1 ISC | NAPIPDL0 ISC |
| 2F | ALPFS7 ISC | ALPFS6 ISC | ALPFS5 ISC | ALPFS4 ISC | ALPFS3 ISC | ALPFS2 ISC | ALPFS1 ISC | ALPFS0 ISC |
| 30 | APPLS7 ISC | APPLS6 ISC | APPLS5 ISC | APPLS4 ISC | APPLS3 ISC | APPLS2 ISC | APPLS1 ISC | APPLS0 ISC |
| 31 | APPLIPS7 ISC | APPLIPS6 ISC | APPLIPS5 ISC | APPLIPS4 ISC | APPLIPS3 ISC | APPLIPS2 ISC | APPLIPS1 ISC | APPLIPS0 ISC |
| 32 | ALPFIPS7 ISC | ALPFIPS6 ISC | ALPFIPS5 ISC | ALPFIPS4 ISC | ALPFIPS3 ISC | ALPFIPS2 ISC | ALPFIPS1 ISC | ALPFIPS0 ISC |
| 33 | VINDELS5 ISC | VINDELS4 ISC | VINDELS3 ISC | VINDELS2 ISC | VINDELS1 ISC | VINDELS0 ISC | VINPOLS ISC | HINPOLS ISC |
| 34 | NALIPS6 ISC | NALIPS5 ISC | NALIPS4 ISC | NALIPS3 ISC | NALIPS2 ISC | NALIPS1 ISC | NALIPS0 ISC | CHRFORS VHCOM |
| 35 | HOUTDEL7 OSC | HOUTDEL6 OSC | HOUTDEL5 OSC | HOUTDEL4 OSC | HOUTDEL3 OSC | HOUTDEL2 OSC | HOUTDEL1 OSC | HOUTDEL0 OSC |
| 36 | NALOPD7 OSC | NALOPD6 OSC | NALOPD5 OSC | NALOPD4 OSC | NALOPD3 OSC | NALOPD2 OSC | NALOPD1 OSC | NALOPD0 OSC |
| 37 | x | ALPFOPD6 OSC | ALPFOPD5 OSC | ALPFOPD4 OSC | ALPFOPD3 OSC | ALPFOPD2 OSC | ALPFOPD1 OSC | ALPFOPD0 OSC |
| 38 | LPFOP7 OSC | LPFOP6 OSC | LPFOP5 OSC | LPFOP4 OSC | LPFOP3 OSC | LPFOP2 OSC | LPFOP1 OSC | LPFOP0 OSC |
| 39 | NAPOPD7 OSC | NAPOPD6 OSC | NAPOPD5 OSC | NAPOPD4 OSC | NAPOPD3 OSC | NAPOPD2 OSC | NAPOPD1 OSC | NAPOPD0 OSC |
| 3A | HORPOSM7 OSC | HORPOSM6 OSC | HORPOSM5 OSC | HORPOSM4 OSC | HORPOSM3 OSC | HORPOSM2 OSC | HORPOSM1 OSC | HORPOSM0 OSC |
| 3B | HORPOSS7 OSC | HORPOSS6 OSC | HORPOSS5 OSC | HORPOSS4 OSC | HORPOSS3 OSC | HORPOSS2 OSC | HORPOSS1 OSC | HORPOSS0 OSC |
| 3C | VERPOSM7 OSC | VERPOSM6 OSC | VERPOSM5 OSC | VERPOSM4 OSC | VERPOSM3 OSC | VERPOSM2 OSC | VERPOSM1 OSC | VERPOSM0 OSC |
| 3D | VERPOSS7 OSC | VERPOSS6 OSC | VERPOSS5 OSC | VERPOSS4 OSC | VERPOSS3 OSC | VERPOSS2 OSC | VERPOSS1 OSC | VERPOSS0 OSC |
| 3E | x | HORWIDTHM6 OSC | HORWIDTHM5 OSC | HORWIDTHM4 OSC | HORWIDTHM3 OSC | HORWIDTHM2 OSC | HORWIDTHM1 OSC | HORWIDTHM0 OSC |
| 3F | HORWIDTHS7 OSC | HORWIDTHS6 OSC | HORWIDTHS5 OSC | HORWIDTHS4 OSC | HORWIDTHS3 OSC | HORWIDTHS2 OSC | HORWIDTHS1 OSC | HORWIDTHS0 OSC |

| | | | | | | | | |
|----|-------------------|-------------------|-------------------|-------------------|--------------------|---------------------|-------------------|-------------------|
| 40 | x | VERWIDTHM6 OSC | VERWIDTHM5 OSC | VERWIDTHM4 OSC | VERWIDTHM3 OSC | VERWIDTHM2 OSC | VERWIDTHM1 OSC | VERWIDTHM0 OSC |
| 41 | VERWIDTHS7 OSC | VERWIDTHS6 OSC | VERWIDTHS5 OSC | VERWIDTHS4 OSC | VERWIDTHS3 OSC | VERWIDTHS2 OSC | VERWIDTHS1 OSC | VERWIDTHS0 OSC |
| 42 | BLANDEL7 OSC | BLANDEL6 OSC | BLANDEL5 OSC | BLANDEL4 OSC | BLANDEL3 OSC | BLANDEL2 OSC | BLANDEL1 OSC | BLANDEL0 OSC |
| 43 | x | APPLOPD6 OSC | APPLOPD5 OSC | APPLOPD4 OSC | APPLOPD3 OSC | APPLOPD2 OSC | APPLOPD1 OSC | APPLOPD0 OSC |
| 44 | BLANLEN7 OSC | BLANLEN6 OSC | BLANLEN5 OSC | BLANLEN4 OSC | BLANLEN3 OSC | BLANLEN2 OSC | BLANLEN1 OSC | BLANLEN0 OSC |
| 45 | PPLP7 OSC | PPLP6 OSC | PPLP5 OSC | PPLP4 OSC | PPLP3 OSC | PPLP2 OSC | PPLP1 OSC | PPLP0 OSC |
| 46 | x | x | x | PPLOP8 OSC | CAPPM1 OSC | CAPPM0 OSC | CAPPS1 OSC | CAPPS0 OSC |
| 47 | x | VERINT6 OSC | VERINT5 OSC | VERINT4 OSC | VERINT3 OSC | VERINT2 OSC | VERINT1 OSC | VERINT0 OSC |
| 48 | x | x | x | STOPMOM3 OSC | STOPMOM2 OSC | STOPMOM1 OSC | STOPMOM0 OSC | RMODE OSC |
| 49 | INTMODE3 OSC | INTMODE2 OSC | INTMODE1 OSC | INTMODE0 OSC | BLANKPOL OSC | ADOPMOM2 OSC | ADOPMOM1 OSC | ADOPMOM0 OSC |
| 4A | x | VOUTFR OSC | HOUTFR OSC | VOUTPOL OSC | HOUTPOL OSC | STOPMOS2 OSC | STOPMOS1 OSC | STOPMOS0 OSC |
| 4B | PRIORMS MUX | FILSEL1 SRCM | FILSEL0 SRCM | MOVPHINV ME | MESMOOTH- ON ME | MENULLUN- FON ME | MEMINMOT1 ME | MEMINMOT0 ME |
| 4C | MEPENUP3 ME | MEPENUP2 ME | MEPENUP1 ME | MEPENUP0 ME | MEADDPEN3 ME | MEADDPEN2 ME | MEADDPEN1 ME | MEADDPEN0 ME |
| 4D | SFMAXTH1 ME | SFMAXTH0 ME | SFMINTH1 ME | SFMINTH0 ME | MEMINTH3 ME | MEMINTH2 ME | MEMINTH1 ME | MEMINTH0 ME |
| 4E | x | x | BVMCON ME | MEMAXTH4 ME | MEMMAXTH3 ME | MEMMAXTH2 ME | MEMMAXTH1 ME | MEMMAXTH0 ME |
| 4F | MEMOHIST3 ME | MEMOHIST2 ME | MEMOHIST1 ME | MEMOHIST0 ME | MENULLPEN3 ME | MENULLPEN2 ME | MENULLPEN1 ME | MENULLPEN0 ME |
| 50 | MEANBP1 ME | MEANBP0 ME | MEANMP1 ME | MEANMP0 ME | MENPTH2 ME | MENPTH1 ME | MENPTH0 ME | MEPERINF ME |
| 51 | MEANRG1 ME | MEANRG0 ME | MEHPERTH2 ME | MEHPERTH1 ME | MEHPERTH0 ME | MEVPERTH2 ME | MEVPERTH1 ME | MEVPERTH0 ME |

| | | | | | | | | |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|
| 52 | x | BVMRES ME | PERPEN2 ME | PERPEN1 ME | PERPEN0 ME | VECDISON SRCM | THYON ME | RESMOV ME |
| 53 | REFRPER1 MC | REFRPER0 MC | MEMOP1 MC | MEMOP0 MC | MASTERON MC | SLAVEON MC | MEMRDM MC | MEMRDS MC |
| 54 | VPAN7 MC | VPAN6 MC | VPAN5 MC | VPAN4 MC | VPAN3 MC | VPAN2 MC | VPAN1 MC | VPAN0 MC |
| 55 | REFRON MC | RSHFTM MC | RSHFTS MC | SHFTSTEP3 MC | SHFTSTEP2 MC | SHFTSTEP1 MC | SHFTSTEP0 MC | MASTSLA MC |
| 56 | PROG_THRES6 MC | PROG_THRES5 MC | PROG_THRES4 MC | PROG_THRES3 MC | PROG_THRES2 MC | PROG_THRES1 MC | PROG_THRES0 MC | MASLSHFT MC |
| 57 | x | x | x | MEMWRS MC | FREEZES MC | WRFLDS MC | ORGMEMS MC | VERRESS MC |
| 58 | x | x | x | MEMWRM MC | FREEZEM MC | WRFLDM MC | ORGMEMM MC | VERRESM MC |
| 59 | MEMMNDTH3 ME | MEMMNDTH2 ME | MEMMNDTH1 ME | MEMMNDTH0 ME | MENVRTH3 ME | MENVRTH2 ME | MENVRTH1 ME | MENVRTH0 ME |
| 5A | DOUTEN DAC | TWOOUT OFC | DACEN DAC | CORING PK | YBORDERD3 OFC | YBORDERD2 OFC | YBORDERD1 OFC | YBORDERD0 OFC |
| 5B | UBORDERD3 OFC | UBORDERD2 OFC | UBORDERD1 OFC | UBORDERD0 OFC | VBORDERD3 OFC | VBORDERD2 OFC | VBORDERD1 OFC | VBORDERD0 OFC |
| 5C | ASCENTLT11 LTI | ASCENTLT10 LTI | ASCENTCT11 CTI | ASCENTCT10 CTI | COARSD3 CD | COARSD2 CD | COARSD1 CD | COARSD0 CD |
| 5D | BCOF3 PK | BCOF2 PK | BCOF1 PK | BCOF0 PK | HCOF3 PK | HCOF2 PK | HCOF1 PK | HCOF0 PK |
| 5E | CHROM_AMP DAC | THRESY_UP1 LTI | THRESY_UP0 LTI | THRESC1 CTI | THRESC0 CTI | THRESY2 LTI | THRESY1 LTI | THRESY0 LTI |
| 5F | x | CLKMDEN PLLD | CLKOUTON PLLD | PLLOFF PLLD | PLLDRA3 PLLD | PLLDRA2 PLLD | PLLDRA1 PLLD | PLLDRA0 PLLD |
| 60-77 | x | x | x | x | x | x | x | x |
| 78 | SLAA7 LBD | SLAA6 LBD | SLAA5 LBD | SLAA4 LBD | SLAA3 LBD | SLAA2 LBD | SLAA1 LBD | SLAA0 LBD |
| 79 | ELAA7 LBD | ELAA6 LBD | ELAA5 LBD | ELAA4 LBD | ELAA3 LBD | ELAA2 LBD | ELAA1 LBD | ELAA0 LBD |
| 7A | NOISEME4 TSNR | NOISEME3 TSNR | NOISEME2 TSNR | NOISEME1 TSNR | NOISEME0 TSNR | VERSION2 I°C | VERSION1 I°C | VERSION0 I°C |

| | | | | | | | | |
|----|----------|----------|------------|-----------|-----------------|-----------------|---------------|----------------------------|
| 7B | x | x | x | x | STATUS_SLAA LBD | STATUS_ELAA LBD | RELY LBD | TVMODEM ISC |
| 7C | x | x | x | x | x | x | NMSTATUS TSNR | LBDSTATUS LBD |
| 7D | x | x | x | x | x | x | x | TVMODES ISC |
| 7E | MOVMO ME | MOVPH ME | GMOTION ME | MOVTYP ME | MEMSTAT3 ME | MEMSTAT2 ME | MEMSTAT1 ME | MEMSTAT0 ME |
| 7F | x | x | x | x | x | x | x | SHIFTACT MC |
| 80 | x | x | x | x | x | x | x | VIMSTATUS I ² C |
| 81 | x | x | x | x | x | x | x | VISSTATUS I ² C |
| 82 | x | x | x | x | x | x | x | OSSTATUS I ² C |

x = don't care

ISC - Input sync controller block

IFC - Input format conversion block

OSC - Output sync controller block

OFC - Output format conversion block

LBD - Letter box detection block

VHCOM - Vertical-horizontal compression/expansion block

TSNR - Temporal noise reduction block

ME - Motion estimation block

PK - Peaking

LTI - Luminance transition improvement block

CTI - Chrominance transition improvement block

CD - Coarse Delay block

MC - Memory controller

PLLM - Clock doubling block master

PLLS - Clock doubling block slave

PLLD - Clock doubling block display

I²C Bus block

5.13.4 Detailed description

Default values are underlined.

| Sub address 00 | | |
|----------------|---------|--------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | x | xxx |
| D4 | PLLMOFF | Only for test purposes, do not use in normal mode PLLM (Clock doubling): 1: off <u>0: on</u> |
| D3...D0 | PLLMRA | Only for test purposes, do not use in normal mode PLLM range, only for test purposes [<u>PPLMRA=0</u>] |

| Sub address 01 | | |
|----------------|--------|------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | IPOSYM | Vertical Picture Position in the Memory for Master Picture resolution: 1 line <u>[IPOSYM=0]</u> - upper position |

| Sub address 02 | | |
|----------------|--------|--------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | IPOSXM | Horizontal Picture Position in the Memory for Master Picture resolution: 4 pixel <u>[IPOSXM=0]</u> - left position |

| Sub address 03 | | |
|----------------|---------|--------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | LEBORDM | Amount of left border pixels by horizontal compression master: 4*LEBORDM [<u>LEBORDM=0</u>] |

| Sub address 03 | | |
|----------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D4...D2 | RIBORDM | Amount of right border pixels by horizontal compression master: $4 \cdot \text{RIBORDM}$ [<u>RIBORDM=0</u>] |
| D1...D0 | CHFILM | Chrominance Filter Master channel on/off 11: vertical and horizontal filter on (only valid for DEZHM=DEZVM=0) 10: horizontal filter on (only valid for DEZHM=0) 01: vertical filter on (only valid for DEZVM=0) <u>00: off</u> |

| Sub address 04 | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | DELM | Adjustable delay between luminance and chrominance data master channel: 111:+4 110:+3 101:+2 100:+1 <u>011: 0</u> 010: -1 001: -2 000: -3 |
| D4 | FORCOLM | Force colour master channel 1: on <u>0: off</u> |
| D3...D0 | YBORDERM | Y border value (Yborder(3) Yborder(2) Yborder(1) Yborder(0) 0 0 0 0 = <u>00010000 = 16</u>), YBORDERM defines the 4 MSB's of a 8 bit value |

| Sub address 05 | | |
|----------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | UBORDERM | U border value (Uborder(3) Uborder(2) Uborder(1) Uborder(0) 0 0 0 0 = $10000000 = 128$), UBORDERM defines the 4 MSB's of a 8 bit value |
| D3...D0 | VBORDERM | V border value (Vborder(3) Vborder(2) Vborder(1) Vborder(0) 0 0 0 0 = $10000000 = 128$), VBORDERM defines the 4 MSB's of a 8 bit value |

| Sub address 06 | | |
|----------------|---------|-----------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | UPBORDM | Amount of upper border lines by vertical compression master: [UPBORDM=0] |
| D3...D0 | LWBORDM | Amount of lower border lines by vertical compression master: [LWBORDM=0] |

| Sub address 07 | | |
|----------------|-------|-----------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | INTHM | Interpolation factor for horizontal compression/expansion master: [INTHM(12...5)=64] |

| Sub address 08 | | |
|----------------|-------|-------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D3 | INTHM | Interpolation factor for horizontal compression/expansion master: INTHM(4...0)=0 |

| Sub address 08 | | |
|----------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D2...D0 | DEZHM | Decimation factor for horizontal compression/expansion master: 111: Factor 16 110: Factor 8 101: Factor 4 100: Factor 2 011: not defined 010: not defined 001: Factor 1 000: <u>Bypass</u> |

| Sub address 09 | | |
|----------------|-------|----------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | INTVM | Interpolation factor for vertical compression master: INTVM+512 [INTVM(8...1)=0] |

| Sub address 0A | | |
|----------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | INTVM | Interpolation factor for vertical compression master: INTVM+512 [INTVM(0)=0] |
| D6...D4 | DEZVM | Decimation factor for vertical compression master: 111: Factor 16 110: Factor 8 101: Factor 4 100: Factor 2 011: not defined 010: not defined 001: Factor 1 000: <u>Bypass</u> |

| Sub address 0A | | |
|----------------|--------|--------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D3...D2 | YPEAKM | Vertical peaking factor for luminance signal master: 11: Factor 4 10: Factor 2 01: Factor 1 <u>00: off</u> |
| D1...D0 | CPEAKM | Vertical peaking factor for chrominance signal master: 11: Factor 4 10: Factor 2 01: Factor 1 <u>00: off</u> |

| Sub address 0B | | |
|----------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6...D5 | FORMATM | Input format master: <u>11: full CCIR 656</u> 10: CCIR 656 only data, H- and V-sync according CCIR656 01: CCIR 656 only data, H- and V-sync according PAL/NTSC 00: 4:2:2 |
| D4 | FIEINVM | Field polarity inversion master: 1: Field A=1, Field B=0 <u>0: Field A=0, Field B=1</u> |
| D3 | VCRMDEM | Input filtering of the incoming field signal master: <u>1: on</u> 0: off |
| D2...D1 | NAPIPPHM (LSBs of NAPLIPM) | Number of not active pixels from external HINM to the input data in system clocks of CLKM: Distance(HINM to input data) = (NAPIPDLM*4+NAPIPPHM+8) <u>[NAPIPPHM = 0]</u> |
| D0 | TWOINM | Chrominance input format master: <u>1: 2's complement input (-128...127)</u> 0: unsigned input (0...255) inside the SDA 9415 the data are always processed as unsigned data |

| Sub address 0C | | |
|----------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | NAPIPDLM (MSBs of NAPLIPM) | Number of not active pixels from HINM to the input data in system clocks of CLKM: Distance(HINM to input data) = (4 * NAPIPDLM + NAPIPPHM + 8) [NAPIPDLM= 0] |

| Sub address 0D | | |
|----------------|-------|-------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | ALPFM | Number of active lines per field after vertical compression master: Active lines = ALPFM * 2 [ALPFM=144] |

| Sub address 0E | | |
|----------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | APPLM | Number of active pixels per line in the input data stream after horizontal expansion/compression in system clocks of CLKM: Active pixels = APPLM*8 [APPLM = 180] |

| Sub address 0F | | |
|----------------|---------|----------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | APPLIPM | Number of active pixels per line in the input data stream in system clocks of CLKM: Active pixels = APPLIPM*8 [APPLIPM = 180] |

| Sub address 10 | | |
|----------------|---------|---------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | ALPFIPM | Number of active lines per field in the input data stream master: Active lines = ALPFIPM * 2 [ALPFIPM=144] |

| Sub address 11 | | |
|----------------|---------|--------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D2 | VINDELM | VINM input delay: Delay(VINM to internal V-sync) = (128 * VINDELM + 1)*Tclkm [VINDELM = 0] |
| D1 | VINPOLM | VINM polarity: 1: low active 0: high active |
| D0 | HINPOLM | HINM polarity: 1: low active 0: high active |

| Sub address 12 | | |
|----------------|-------------|-------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6...D2 | NALIPM | Number of not active lines per field in the input data stream master: Not active lines = NALIPM+3 [NALIPM= 20] |
| D1...D0 | CHRFOR M | Chrominance Format Master Channel: 11: not defined 10: reserved 01: 4:2:0 00: 4:1:1 |

| Sub address 14 | | |
|----------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D6 | x | xx |
| D5...D1 | NMLINE | Line for noise measurement (only valid for NMALG=1) [<u>NMLINE</u> = 4] |
| D0 | NMALG | Noise measurement algorithm: 1: <u>measurement during vertical blanking period (line can be defined by NMLINE)</u> 0: measurement in the active picture |

| Sub address 15 | | |
|----------------|--------|-------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | TNRCLY | Temporal noise reduction of luminance: classification <u>1111: slight noise reduction</u> : 0000: strong noise reduction |
| D3...D0 | TNRCLC | Temporal noise reduction of chrominance: classification <u>1111: slight noise reduction</u> : 0000: strong noise reduction |

| Sub address 16 | | |
|----------------|--------|----------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | TNRKOY | Temporal noise reduction of luminance: Vertical shift of the motion detector characteristic [<u>TNRKOY=0</u>] |
| D3...D0 | TNRKOC | Temporal noise reduction of chrominance: Vertical shift of the motion detector characteristic [<u>TNRKOC=0</u>] |

| Sub address 17 | | |
|----------------|--------|-----------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | TNRVAY | Fixed K-factor for temporal noise reduction of luminance [TNRVAY = 15] |
| D3...D0 | TNRVAC | Fixed K-factor for temporal noise reduction of chrominance [TNRVAC = 15] |

| Sub address 18 | | |
|----------------|--------|------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | TNRSEL | Motion detection of temporal noise reduction of chrominance: <u>1: separate motion detector</u> 0: luminance motion detector |
| D6...D1 | TNRHOY | Temporal noise reduction of luminance: Horizontal shift of the motion detector characteristic [TNRHOY=0] |
| D0 | TNRFIY | Fixed K-factor switch for temporal noise reduction of luminance: <u>1: off</u> 0: on |

| Sub address 19 | | |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6...D1 | TNRHOC | Temporal noise reduction of chrominance: Horizontal shift of the motion detector characteristic [TNRHOC=0] |
| D0 | TNRFIC | Fixed K-factor switch for temporal noise reduction of chrominance: <u>1: off</u> 0: on |

| Sub address 1A | | |
|----------------|--------|--------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | SNRON | Spatial noise reduction of luminance: 1: enabled 0: disabled |
| D6 | PANAON | Horizontal panorama mode: 1: on 0: off |
| D5...D2 | PANAST | Gradient of horizontal panorama mode: PANAST+1 [PANAST=7] |
| D1 | NRON | Temporal Noise Reduction of Luminance and Chrominance On (SRC-Mode) 1: enabled 0: disabled |
| D0 | DTNRON | Temporal Noise Reduction of Luminance (SRC-Mode) 1: field based 0: frame based |

| Sub address 1B | | |
|----------------|--------|--------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | OPDELM | Output processing delay master: Delay(VINM to OPSTARTM) = (OPDELM + 1) * Tline [OPDELM = 170] |

| Sub address 1C | | |
|----------------|----------|-------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D2 | TH_DN_BN | Letter Box Detection: Darkness Brightness threshold [TH DN BN = 15] |
| D1...D0 | TH_LB | Letter Box Detection: Letter Box threshold (MSBs) [TH LB(5...4) = 0] |

| Sub address 1D | | |
|----------------|--------|--------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | TH_LB | Letter Box Detection: Letter Box threshold (LSBs) [TH_LB(3...0) = 12] |
| D3...D0 | TH_ALB | Letter Box Detection: Amount of letter box threshold [TH_ALB = 6] |

| Sub address 1E | | |
|----------------|-------|-------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6...D0 | TH_AA | Letter Box Detection: Active Area threshold [TH_AA = 50] |

| Sub address 1F | | |
|----------------|----------|------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | TH_MUNSL | Letter Box Detection: Maximum length of insecure threshold [TH_MUNSL = 5] |
| D3...D0 | TH_AUNS | Letter Box Detection: Amount of letter box and insecure threshold [TH_AUNS = 7] |

| Sub address 20 | | |
|----------------|----------|----------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | x | xxx |
| D4...D1 | TH_MA_AA | Letter Box Detection: Maximum amount of active area threshold [TH_MA_AA = 14] |

| Sub address 20 | | |
|----------------|-------|-----------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D0 | VOLBD | Letter Box Detection: Makes the result of letter box detection visible on screen 1: on 0: off |

| Sub address 22 | | |
|----------------|---------|-----------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | x | xxx |
| D4 | PLLSOFF | Only for test purposes, do not use in normal mode PLLS (Clock doubling): 1: off 0: on |
| D3...D0 | PLLSRA | Only for test purposes, do not use in normal mode PLLS range, only for test purposes [PPLSRA=0] |

| Sub address 23 | | |
|----------------|--------|----------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | IPOSYS | Vertical Picture Position in the Memory for Slave Picture resolution: 1 line [IPOSYS=0] - upper position |

| Sub address 24 | | |
|----------------|--------|------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | IPOSXS | Horizontal Picture Position in the Memory for Slave Picture resolution: 4 pixel [IPOSXS=0] - left position |

| Sub address 25 | | |
|----------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | LEBORDS | Amount of left border pixels by horizontal compression slave: 4*LEBORDS [<u>LEBORDS=0</u>] |
| D4...D2 | RIBORDS | Amount of right border pixels by horizontal compression slave: 4*RIBORDS [<u>RIBORDS=0</u>] |
| D1...D0 | CHFILS | Chrominance Filter Slave channel on/off 11: vertical and horizontal filter on (only valid for DEZHS=DEZVS=0) 10: horizontal filter on (only valid for DEZHS=0) 01: vertical filter on (only valid for DEZVS=0) <u>00: off</u> |

| Sub address 26 | | |
|----------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | DELS | Adjustable delay between luminance and chrominance data slave channel: 111:+4 110:+3 101:+2 100:+1 <u>011: 0</u> 010: -1 001: -2 000: -3 |
| D4 | FORCOLS | Force colour slave channel 1: on <u>0: off</u> |
| D3...D0 | YBORDERS | Y border value (Yborder(3) Yborder(2) Yborder(1) Yborder(0) 0 0 0 = <u>00010000 = 16</u>), YBORDERS defines the 4 MSB's of a 8 bit value |

| Sub address 27 | | |
|-----------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | UBORDERS | U border value (Uborder(3) Uborder(2) Uborder(1) Uborder(0) 0 0 0 0 = <u>10000000</u> = 128), UBORDERS defines the 4 MSB's of a 8 bit value |
| D3...D0 | VBORDERS | V border value (Vborder(3) Vborder(2) Vborder(1) Vborder(0) 0 0 0 0 = <u>10000000</u> = 128), VBORDERS defines the 4 MSB's of a 8 bit value |

| Sub address 28 | | |
|-----------------------|-------------|--------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | UPBORDS | Amount of upper border lines by vertical compression master: [UPBORDS=0] |
| D3...D0 | LWBORDS | Amount of lower border lines by vertical compression master: [LWBORDS=0] |

| Sub address 29 | | |
|-----------------------|-------------|-------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | INTHS | Interpolation factor for horizontal compression/expansion slave: [INTHS(12...5)=64] |

| Sub address 2A | | |
|-----------------------|-------------|-----------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D3 | INTHS | Interpolation factor for horizontal compression/expansion slave: [INTHS(4...0)=0] |

| Sub address 2A | | |
|----------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D2...D0 | DEZHS | Decimation factor for horizontal compression/expansion slave: 111: Factor 16 110: Factor 8 101: Factor 4 100: Factor 2 011: not defined 010: not defined 001: Factor 1 000: Bypass |

| Sub address 2B | | |
|----------------|-------|------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | INTVS | Interpolation factor for vertical compression slave: INTVS+512 [INTVS(8...1)=0] |

| Sub address 2C | | |
|----------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | INTVS | Interpolation factor for vertical compression slave: INTVS+512 [INTVS(0)=0] |
| D6...D4 | DEZVS | Decimation factor for vertical compression slave: 111: Factor 16 110: Factor 8 101: Factor 4 100: Factor 2 011: not defined 010: not defined 001: Factor 1 000: Bypass |

| Sub address 2C | | |
|----------------|--------|-------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D3...D2 | YPEAKS | Vertical peaking factor for luminance signal slave: 11: Factor 4 10: Factor 2 01: Factor 1 <u>00: off</u> |
| D1...D0 | CPEAKS | Vertical peaking factor for chrominance signal slave: 11: Factor 4 10: Factor 2 01: Factor 1 <u>00: off</u> |

| Sub address 2D | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | SLAVECON | Slave channel connection: 1: Slave channel connected <u>0: Slave channel not connected</u> |
| D6...D5 | FORMATS | Input format slave: <u>11: full CCIR 656</u> 10: CCIR 656 only data, H- and V-sync according CCIR656 01: CCIR 656 only data, H- and V-sync according PAL/NTSC 00: 4:2:2 |
| D4 | FIEINVS | Field polarity inversion slave: 1: Field A=1, Field B=0 <u>0: Field A=0, Field B=1</u> |
| D3 | VCRModes | Input filtering of the incoming field signal slave: <u>1: on</u> 0: off |

| | | |
|---------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D2...D1 | NAPIPPHS (LSBs of NAPLIPS) | Number of not active pixels from external HINS to the input data in system clocks of CLKS: Distance(HINS to input data) = (NAPIPDLS*4+NAPIPPHS+8) [NAPIPPHS = 0] |
| D0 | TWOINS | Chrominance input format slave: 1: 2's complement input (-128...127) 0: unsigned input (0...255) inside the SDA 9415 the data are always processed as unsigned data |

| Sub address 2E | | |
|----------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | NAPIPDLS (MSBs of NAPLIPS) | Number of not active pixels from HINS to the input data in system clocks of CLKS: Distance(HINS to input data) = (4 * NAPIPDLS + NAPIPPHS + 8) [NAPIPDLS= 0] |

| Sub address 2F | | |
|----------------|-------|------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | ALPFS | Number of active lines per field after vertical compression slave: Active lines = ALPFS * 2 [ALPFS=144] |

| Sub address 30 | | |
|----------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | APPLS | Number of active pixels per line in the input data stream after horizontal expansion/compression in system clocks of CLKS: Active pixels = APPLS*8 [APPLS = 180] |

| Sub address 31 | | |
|----------------|---------|----------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | APPLIPS | Number of active pixels per line in the input data stream in system clocks of CLKS: Active pixels = APPLIPS*8 [APPLIPS = 180] |

| Sub address 32 | | |
|----------------|---------|--------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | ALPFIPS | Number of active lines per field in the input data stream slave: Active lines = ALPFIPS * 2 [ALPFIPS=144] |

| Sub address 33 | | |
|----------------|---------|--------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D2 | VINDELS | VINS input delay: Delay(VINS to internal V-sync) = (128 * VINDELS + 1)*Tclks [VINDELS = 0] |
| D1 | VINPOLS | VINS polarity: 1: low active 0: high active |
| D0 | HINPOLS | HINS polarity: 1: low active 0: high active |

| Sub address 34 | | |
|----------------|------|----------|
| Bit | Name | Function |
| D7...D6 | x | xx |

| Sub address 34 | | |
|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D1 | NALIPS | Number of not active lines per field in the input data stream slave: Not active lines = NALIPS+PD [NALIPS= 20] Enables 16x9 format adjustment for PIP display |
| D0 | CHRFORS | Chrominance format slave channel: 1: 4:2:0 0: 4:1:1 |

| Sub address 35 | | |
|----------------|---------|------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | HOUTDEL | Horizontal delay of HOUT and VOUT signal in clocks of CLKD: Delay = 4*HOUTDEL [HOUTDEL = 0] |

| Sub address 36 | | |
|----------------|--------|-------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | NALOPD | Number of not active lines per output frame in the output data stream: Not active lines = 2*(NALOPD+1) [NALOPD = 22] |

| Sub address 37 | | |
|----------------|---------|--------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | | x |
| D6...D0 | ALPFOPD | Number of active lines per output frame: Active lines = 8 * ALPFOPD [ALPFOPD= 72] |

| Sub address 38 | | |
|----------------|-------|--------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | LPFOP | Number of lines per output frame (only valid for VOUTFR=1): Number of lines = $4 * LPFOP + 1$ [$LPFOP = 156$] |

| Sub address 39 | | |
|----------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | NAPOPD | Number of not active pixels from external HOUT to the first active pixel of the output data stream (when HOUTDEL = 0) in system clocks of X1/CLKD: Distance(HOUT to output data) = $(4 * NAPOPD)$ [$NAPOPD = 0$] |

| Sub address 3A | | |
|----------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | HORPOSM | Number of pixels from the first active pixel of the main channel to the first active pixel of the master channel in system clocks of X1/CLKD: Number of pixels = $(4 * HORPOSM)$ [$HORPOSM = 0$] |

| Sub address 3B | | |
|----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | HORPOSS | Number of pixels from the first active pixel of the main channel to the first active pixel of the slave channel in system clocks of X1/CLKD: Number of pixels = $(4 * HORPOSS)$ [$HORPOSS = 0$] |

| Sub address 3C | | |
|----------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | VERPOSM | Number of lines from the first active line of the main channel to the first active line of the master channel per output frame: Number of lines = VERPOSM [VERPOSM = 0] |

| Sub address 3D | | |
|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | VERPOSS | Number of lines from the first active line of the main channel to the first active line of the slave channel per output frame: Number of lines = VERPOSS [VERPOSS = 0] |

| Sub address 3E | | |
|----------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6...D0 | HORWIDTHM | Number of active pixels per line of the master channel in system clocks of X1/CLKD: Active pixels = 8 * HORWIDTHM [HORWIDTHM = 90] |

| Sub address 3F | | |
|----------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | HORWIDTHS | Number of active pixels per line of the slave channel in system clocks of X1/CLKD: Active pixels = 4 * HORWIDTHS [HORWIDTHS = 180] |

| Sub address 40 | | |
|----------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | | x |
| D6...D0 | VERWIDTHM | Number of active lines per field of the master channel per output frame: Active lines = $8 * \text{VERWIDTHM}$ [<u>VERWIDTHM = 72</u>] |

| Sub address 41 | | |
|----------------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | VERWIDTHS | Number of active lines per field of the master channel per output frame: Active lines = $4 * \text{VERWIDTHS}$ [<u>VERWIDTHS = 144</u>] |

| Sub address 42 | | |
|----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | BLANDEL | Number of pixels from external HOUT to the active edge of the BLANK signal in system clocks of X1/CLKD: Number of pixels = $(8 * (\text{BLANDEL} \text{ div } 4) + \text{BLANDEL} \text{ mod } 3)$ [<u>BLANDEL = 0</u>] |

| Sub address 43 | | |
|----------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | | x |
| D6...D0 | APPLOPD | Number of active pixels per line (including coloured border values and data) in the output data stream in system clocks of X1/CLKD: Active pixels = $8 * \text{APPLOPD}$ [<u>APPLOPD = 90</u>] |

| Sub address 44 | | |
|----------------|---------|-------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | BLANLEN | Length of the signal BLANK in system clocks of X1/CLKD: Length = 4 * BLANLEN [BLANLEN = 180] |

| Sub address 45 | | |
|----------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | PPLOP(7...0) | Number of pixels between two output H-syncs HOUT (only valid for HOUTFR=1) in system clocks of X1/CLKD (Bit 7 to 0): Number of pixels = 2 * PPLOP [PPLOP(7...0) = 176] |

| Sub address 46 | | |
|----------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | x | xxx |
| D4 | PPLOP(8) | Number of pixels between two output H-syncs HOUT (only valid for HOUTFR=1) in system clocks of X1/CLKD (Bit 8): Number of pixels = 2 * PPLOP [PPLOP(8) = 1] |
| D3...D2 | CAPPM | Reduces the active pixels per line of the master channel (HORWIDTHM) at the output side = $8 * HORWIDTHM - 2 * k$: k = 24: CAPPM = 11 16: CAPPM = 10 8: CAPPM = 01 0: CAPPM = 00 |
| D1...D0 | CAPPS | Reduces the active pixels per line of the slave channel (HORWIDTHS) at the output side = $4 * HORWIDTHS - 2 * k$: k = 24: CAPPS = 11 16: CAPPS = 10 8: CAPPS = 01 0: CAPPS = 00 |

| Sub address 47 | | |
|----------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | | x |
| D6...D0 | VERINT | Vertical expansion factor: <u>127: no vertical expansion</u> : 85: vertical expansion with factor 1.5 : 63: vertical expansion with factor 2 : |

| Sub address 48 | | |
|----------------|---------|-----------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | x | xxx |
| D4...D1 | STOPMOM | Static operation mode for master channel [<u>STOPMOM = 0</u>] |
| D0 | RMODE | Raster mode: 1: progressive <u>0: interlaced</u> |

| Sub address 49 | | |
|----------------|----------|---------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | INTMODE | Free programmable INTERLACED signal for AC coupled deflections [<u>INTMODE = 0</u>] |
| D3 | BLANKPOL | BLANK polarity: 1: low active <u>0: high active</u> |
| D2...D0 | ADOPMOM | Adaptive operation mode of master channel [<u>ADOPMOM=0</u>] |

| Sub address 4A | | |
|----------------|---------|-----------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6 | VOUTFR | VOUT generator: 1: freerunning-mode <u>0: locked-mode</u> |
| D5 | HOUTFR | HOUT generator 1: freerunning-mode <u>0: locked-mode</u> |
| D4 | VOUTPOL | VOUT polarity: 1: low active <u>0: high active</u> |
| D3 | HOUTPOL | HOUT polarity: 1: low active <u>0: high active</u> |
| D2...D0 | STOPMOS | Static operation mode for slave channel [<u>STOPMOS = 0</u>] |

| Sub address 4B | | |
|----------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | PRIORMS | Priority of master or slave channel: 1: <u>Master channel priority</u> 0: Slave channel priority |
| D6...D5 | FILSEL | Filter select for VDU interpolation 11: Improved median based interfield interpolation (SRC) 10: median based interfield interpolation 01: linear INTRAFIELD interpolation (SSC and MUP mode) <u>00: linear INTERFIELD interpolation</u> |
| D4 | MOVPHINV | Inversion of internal MOVPH signal 1: enabled <u>0: disabled</u> |
| D3 | ME-SMOOTHON | Vector smoothing <u>1: on</u> 0: off |

| Sub address 4B | | |
|----------------|--------------|---------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D2 | MENULL-UNFON | Unfiltered null DBD <u>1: on</u> 0: off |
| D1...D0 | MEMINMOT | Minimum vector threshold for film mode and global motion detection 11: 3 10: 2 <u>01: 1</u> 00 :0 |

| Sub address 4C | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | MEPENUP | Penalty for update vectors 1111: 15 1110: 14 : <u>1000: 8</u> : 0001: 1 0000: 0 |
| D3...D0 | MEADDPEN | Additional penalty for non-null vectors 1111: 15 1110: 14 : <u>1000: 8</u> : 0001: 1 0000: 0 |

| Sub address 4D | | |
|----------------|---------|-------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D6 | SFMAXTH | Scale factor for MEMAXTH 11: *64 <u>10: *32</u> 01: *16 00: *8 |
| D5...D4 | SFMINTH | Scale factor for MEMINTH 11: *64 10: *32 01: *16 <u>00: *8</u> |
| D3...D0 | MEMINTH | Threshold for detection of motion in camera mode 1111 : 15 1110 : 14 : <u>0111 : 7</u> : 0001: 1 0000: 0 |

| Sub address 4E | | |
|----------------|---------|-----------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D6 | xx | xx |
| D5 | BVMCON | Vector correction <u>1: on</u> 0: off |
| D4...D0 | MEMAXTH | Threshold for detection of motion in film mode <u>11111 : 31</u> 11110 : 30 : <u>00001: 1</u> 00000: 0 |

| Sub address 4F | | |
|----------------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | MEMOHIST | History length of film mode and global motion detection 1111 : 15 1110 : 14 : <u>0011: 3</u> : 0001: 1 0000: 0 |
| D3...D0 | MENULLPEN | Additional penalty for null vector, if vector length of predictor is greater as MENPTH 1111: 15 1110: 14 : <u>1000: 8</u> : 0001: 1 0000: 0 |

| Sub address 50 | | |
|----------------|--------|------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D6 | MEANBP | Penalty for border lines in additional null dbd 11: *4 10: *2 <u>01: *1</u> 00: *0 |
| D5...D4 | MEANMP | Penalty for middle lines in additional null dbd 11: *8 10: *4 <u>01: *2</u> 00: *1 |

| Sub address 50 | | |
|----------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D3..D1 | MENPTH | Minimum vector length for null dbd penalty 111: off 110: 24 101: 20 100: 16 <u>011: 12</u> 010: 8 001: 4 000: 0 |
| D0 | MEPERINF | Influence of periodicity on 1: update vector length <u>0: update vector penalty</u> |

| Sub address 51 | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D6 | MEANRG | Range of middle lines in additional null dbd 11: 10 lines 10: 8 lines <u>01: 6 lines</u> 00: 4 lines |
| D5...D3 | MEHPERTH | Threshold for horizontal periodicity detection 111: 112 110: 96 101: 80 <u>100: 64</u> 011: 48 010: 32 001: 16 000: off |

| Sub address 51 | | |
|----------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D2...D0 | MEVPERTH | Threshold for vertical periodicity detection 111: 112 110: 96 101: 80 <u>100: 64</u> 011: 48 010: 32 001: 16 000: off |

| Sub address 52 | | |
|----------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6 | BVMRES | Block vector memory reset 1: All vector memory output values are set to null vector (for scan rate conversion and vector estimation). Corrupt vectors are avoided, suppressed or deleted. This is equal to a reset of the vector memory. <u>0: Use vectors stored in vector memory</u> |
| D5...D3 | PERPEN | Penalty for periodic structures. Reduces estimation errors inside horizontal periodic structures. <u>111: off</u> 110: strong : 011: recommended : 000: slight |

| Sub address 52 | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D2 | VECDISON | Display of vector estimation results in chrominance channel 1: on 0: off If VECDISON is on, the I ² C Bus parameter FILSEL can be used to choose between different display modi: FILSEL: 11: x-vector: v-component; y-vector: u-component 10: x-vector: u-component; y-vector: v-component 01: y-vector: u- and v-component 00: x-vector: u- and v-component |
| D1 | THYON | Time hysteresis for film mode detection on/off: <u>1: on (camera->film: 2*(MEMOHIST+1); film->camera: (MEMOHIST+1)</u> 0: off (2*(MEMOHIST+1)) |
| D0 | RESMOV | Reset of film detection time hysteresis queue 1: Reset: MOVMO=0 (camera mode) <u>0: no reset</u> |

| Sub address 53 | | |
|----------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D6 | REFRPER | Refresh Period of the Memory (REFRON=1; 50 Hz, 625 lines standard) 11: ~4 ms 10: ~5.5 ms 01: ~7 ms <u>00: ~10 ms</u> |
| D5...D4 | MEMOP | Memory Operation Mode 11: not defined 10: MUP-Mode (Multi-Picture) 01: SSC-Mode (Split Screen) <u>00: SRC-Mode (Sample Rate Conversion)</u> |
| D3 | MASTERON | Reading Data of Master Channel <u>1: enabled (master picture is displayed)</u> 0: disabled |

| Sub address 53 | | |
|----------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D2 | SLAVEON | Reading Data of Slave Channel 1: enabled (slave picture is displayed) 0: disabled |
| D1 | MEMRDM | Memory Read Mode Master Channel (SRC-Mode) 1:reading only 1 field memory area for AABB conversion 0:reading both field memory areas for ABAB conversion |
| D0 | MEMRDS | Memory Read Mode Slave Channel (SRC-Mode) 1:reading data in SSC-configuration, 1 or 2 decimated fields, AABB 0:reading data in PIP-configuration (joint line free, ABAB) |

| Sub address 54 | | |
|----------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | VPAN | Vertical Panning -line number indicating the start line of reading for the master channel -defines the displayed part of the picture with activated vertical interpolation [VPAN=0] |

| Sub address 55 | | |
|----------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | REFRON | Refresh On 1: memory refresh activated 0: no memory refresh |
| D6 | RSHFTM | Joint Line Free Display of Master Channel by Shifting the Output Raster Phase (SSC-Mode): <u>Should be set in all operation modes to 1</u> 1: enabled 0: disabled |

| Sub address 55 | | |
|----------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D5 | RSHFTS | Joint Line Free Display of Master and Slave Channel by Shifting the Output Raster Phase (SSC-Mode, RSHFTM=1): <u>Should be set in all operation modes to 1</u> 1: enabled 0: disabled |
| D4...D1 | SHFTSTEP | Increment for Raster Phase Shift per Output Frame (lines) [SHFTSTEP=0100] |
| D0 | MASTSLA | Master / Slave Switch 1: master and slave input signals are exchanged, reset of display raster shift 0: display raster is synchronized to input Master Channel (vertical Sync) |

| Sub address 56 | | |
|----------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D1 | PROG_THRES | Threshold to display progressive PIP without joint lines [PROG_THRES=60] |
| D0 | MASLSHFT | Master / Slave Shift 1: display raster is shifted slave phase to prepare a master/slave switch 0: display raster is synchronized to input Master Channel (vertical Sync) |

| Sub address 57 | | |
|----------------|------|----------|
| Bit | Name | Function |
| D7...D5 | xxx | xxx |

| Sub address 57 | | |
|-----------------------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D4 | MEMWRS | Memory Write Mode Slave Channel (SRC-Mode) - SRC-Mode: 1:writing data in PIP-configuration <u>and</u> additionally in SSC-configuration 0:writing data in <u>PIP-configuration</u> - SSC- and MUP-Mode: 1:768 pixel/line 0:512 pixel/line |
| D3 | FREEZES | Freeze Picture Slave 1: freezed (no writing of slave data) 0: live |
| D2 | WRFLDS | Write Field Slave Channel (only MUP Mode) 1: only A fields are written 0: all fields are written corresponding on actual mode |
| D1 | ORGMEMMS | Data Configuration of the Memory (Slave Channel) 0:slave channel blocked (SRC-Mode, ORGMEMM=1) 1 field (SSC- and MUP-Mode; SRC-Mode, ORGMEMM=0) 1:3 fields PIP (SRC), 2 fields (restricted picture size, SSC and MUP) |
| D0 | VERRESS | Vertical Resolution Slave Channel (only MUP Mode) (ORGMEMMS=1 and WRFLDS=1) 1: frame resolution 0: field resolution |

| Sub address 58 | | |
|-----------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D5 | xxx | xxx |
| D4 | MEMWRM | Memory Write Mode Master Channel - SRC-Mode: no meaning, should be set to '0' - SSC- and MUP-Mode: 0:512 pixel/line 1:768 pixel/line |

| Sub address 58 | | |
|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D3 | FREEZEM | Freeze Picture Master 1: freezed (no writing of master data) <u>0: live</u> |
| D2 | WRFLDM | Write Field Master Channel (only MUP Mode) 1: only A fields are written <u>0: all fields are written corresponding on actual mode</u> |
| D1 | ORGMEMM | Data Configuration of the Memory (Master Channel) <u>1:2 fields (restricted picture size in SSC- and MUP-Mode)</u> 0:1 field |
| D0 | VERRESM | Vertical Resolution Master Channel (MUP Mode) (ORGMEMM=1 and WRFLDM=1) 1: frame resolution <u>0: field resolution</u> |

| Sub address 59 | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | MEMMNDTH | Threshold for switching between the vector activity or the field difference as input for the film mode detection Use field difference as film mode detection input 1111: insensible to motion : 0001: sensible to motion <u>0000: use vector activity as film mode detection input</u> |
| D3...D0 | MENVRTH | Null vector reliability threshold, makes detection of null vector in homegenous areas more reliable. Threshold value to adjust sensibility of null vector reliability: 1111: insensible : 0001: sensible to motion and noise <u>0000: off</u> |

| Sub address 5A | | |
|----------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | DOUTEN | 1: Digital output enabled <u>0: Digital output disabled</u> |
| D6 | TWOOUT | Chrominance output format: 1: 2's complement output (-128...127) <u>0: unsigned output (0...255)</u> inside the SDA 9415 the data are always processed as unsigned data, used in DP, makes only sense for digital output |
| D5 | DACEN | Only for test purposes, do not use in normal mode <u>1: DAC enabled</u> 0: DAC disabled |
| D4 | CORING | 1: coring on <u>0: coring off</u> |
| D3...D0 | YBORDERD | Y border value of display (Yborderd(3) Yborderd(2) Yborderd(1) Yborderd(0) 0 0 0 0 = <u>00010000 = 16</u>), YBORDERD defines the 4 MSB's of a 8 bit value |

| Sub address 5B | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | UBORDERD | U border value of display (Uborderd(3) Uborderd(2) Uborderd(1) Uborderd(0) 0 0 0 0 = <u>10000000 = 128</u>), UBORDERD defines the 4 MSB's of a 8 bit value |
| D3...D0 | VBORDERD | V border value of display (Vborderd(3) Vborderd(2) Vborderd(1) Vborderd(0) 0 0 0 0 = <u>10000000 = 128</u>), VBORDERD defines the 4 MSB's of a 8 bit value |

| Sub address 5C | | |
|----------------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D6 | ASCENTLTI | Defines slope of DLTl gain function 00: 1/2 <u>01: 1</u> 10: 2 11: 4 |
| D5...D4 | ASCENTCTI | Defines slope of DCTl gain function 00: 1/2 <u>01: 1</u> 10: 2 11: 4 |
| D3...D0 | COARSDEL | Delay of the luminance signal in relation to the chrominance signal in 2*CLKD clocks: 1111: +7 1110: +6 : <u>1000: +0</u> : 0001: -7 0000: -8 |

| Sub address 5D | | |
|----------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | BCOF | Defines the band pass filter adjustments 0000: 0 0001: 1/4 : . <u>0100: 1</u> : : . 1100 12/4 1101 14/4 1110 16/4 1111 20/4 |
| D3...D0 | HCOF | Defines the high pass filter adjustments 0000: 0 0001: 1/4 : . <u>0100: 1</u> : : . 1100 12/4 1101 14/4 1110 16/4 1111 20/4 |

| Sub address 5E | | |
|----------------|-----------|-----------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | CHROM_AMP | Chrominance amplification factor adjustment for DAC output 1: amplification factor 2 <u>0: amplification factor 1</u> |

| Sub address 5E | | |
|----------------|-----------|-----------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D6...D5 | THRESY_UP | Defines the upper threshold for luminance 00: 255 (no upper threshold) 01: 32 10: 128 <u>11: 64</u> |
| D4...D3 | THRESC | Defines the threshold for chrominance 00: 255 (DCTI OFF) 01: 4 <u>10: 8</u> 11: 12 |
| D2...D0 | THRESY | defines the threshold for luminance 000: 255 (DLTI OFF) 001: 4 010: 8 <u>011: 12</u> 100: 16 : 111: 28 |

| Sub address 5F | | |
|----------------|----------|--------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | x | x |
| D6 | CLKMDEN | CLKMDEN 1: X1/CLKD <u>0: CLKM</u> |
| D5 | CLKOUTON | CLKOUTON <u>1: enabled</u> 0: disabled |
| D4 | PLLDOFF | Only for test purposes, do not use in normal mode PLLM (Clock doubling): 1: off <u>0: on</u> |
| D3...D0 | PLLDRA | Only for test purposes, do not use in normal mode PLLM range, only for test purposes [PPLDRA=0] |

| Sub address 78 | | |
|----------------|------|------------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | SLAA | Letter box detection: First Line of Active Area = 2 * SLAA |

| Sub address 79 | | |
|----------------|------|----------------------------------------------------------|
| Bit | Name | Function |
| D7...D0 | ELAA | Letter box detection: End Line of Active Area = 2 * ELAA |

| Sub address 7A | | |
|----------------|---------|--------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D3 | NOISEME | Noise level of the input signal: 0 (no noise), ..., 30 (strong noise) [31 (strong noise or measurement failed)] |
| D2...D0 | VERSION | Version of SDA 94XX family: 000: SDA 9400 001: SDA 9401 010: SDA 9402 100: SDA 9410 |

| Sub address 7B | | |
|----------------|-------------|----------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D4 | xxxx | xxxx |
| D3 | Status_SLAA | Letter box detection: Status of SLAA 1: SLAA is reliable 0: SLAA is not reliable |
| D2 | Status_ELAA | Letter box detection: Status of ELAA 1: ELAA is reliable 0: ELAA is not reliable |

| Sub address 7B | | |
|-----------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D1 | RELY | Letter box detection: Reliability signal 1: All values determined by the Letter Box detection algorithm are reliable 0: One or more values determined by the Letter Box detection are not reliable |
| D0 | TVMODEM | TV mode of the input signal master 1: NTSC 0: PAL |

| Sub address 7C | | |
|-----------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D2 | xxxxxx | xxxxxx |
| D1 | NMSTATUS | Status bit for noise measurement I ² C Bus parameter 1: New value of NOISEME available 0: NOISEME has not been updated |
| D0 | LBDSTATUS | Status bit for letter box detection I ² C Bus parameter 1: New values of Letter Box Detection algorithm available 0: Values of Letter Box Detection has not been updated |

| Sub address 7D | | |
|-----------------------|-------------|--------------------------------------------------------|
| Bit | Name | Function |
| D7...D1 | xxxxxxx | xxxxxxx |
| D0 | TVMODES | TV mode of the input signal slave 1: NTSC 0: PAL |

| Sub address 7E | | |
|----------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7 | MOVMO | Film mode 1: film mode 0: camera mode |
| D6 | MOVPH | Film mode phase 1 - An+1 and Bn has the same phase 0 - An and Bn has the same phase |
| D5 | GMOTION | Global motion detection 1: if no STILL scene is detected (minimum is: 1 field in motion of 32 fields in order) 0: if STILL scene is detected (32 fields in order without motion) |
| D4 | MOVTYP | Film mode type 1: NTSC film mode source with 24 motion phases per second (2-3 pull down) 0: PAL film mode source with 25 motion phases per second |
| D3...0 | MEMSTAT | Statistics about motion blocks |

| Sub address 7F | | |
|----------------|----------|----------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D1 | xxxxxxx | xxxxxxx |
| D0 | SHIFTECT | Shifting of Display Raster Phase Active 1: phase shift in progress 0: phase shift not active |

| Sub address 80 | | |
|----------------|---------|----------|
| Bit | Name | Function |
| D7...D1 | xxxxxxx | xxxxxxx |

| Sub address 80 | | |
|----------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D0 | VIMSTATUS | Status bit for sub addresses, which will be made valid by VINM 0: New write or read cycle can start 1: No new write or read cycle can start |

| Sub address 81 | | |
|----------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D1 | xxxxxxx | xxxxxxx |
| D0 | VISSTATUS | Status bit for sub addresses, which will be made valid by VINS 0: New write or read cycle can start 1: No new write or read cycle can start |

| Sub address 82 | | |
|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit | Name | Function |
| D7...D1 | xxxxxxx | xxxxxxx |
| D0 | OSSTATUS | Status bit for sub addresses, which will be made valid by OPSTARTM 0: New write or read cycle can start 1: No new write or read cycle can start |

Electrical Characteristics

6 Electrical Characteristics

6.1 Absolute maximum ratings

| Parameter | Symbol | Min | Max | Unit | Remark |
|------------------------------|-----------|-------|--------------|------|------------------------------------------------------------------------------------------|
| Operating Temperature | T_A | 0 | 70 | °C | |
| Storage Temperature | T_{stg} | -65 | 125 | °C | |
| Junction Temperature | T_J | | 125 | °C | |
| Soldering Temperature | T_S | | 260 | °C | |
| Soldering Time | t_s | | 10 | s | |
| Input Voltage | V_I | -0.3 | $V_{DD}+0.3$ | V | not valid for I ² C Bus pins |
| Output Voltage | V_Q | -0.3 | $V_{DD}+0.3$ | V | not valid for I ² C Bus pins |
| Input Voltage | V_I | -0.3 | 5.5 | V | I ² C Bus pins only |
| Output Voltage | V_O | -0.3 | 5.5 | V | I ² C Bus pins only |
| Supply Voltages | V_{DD} | -0.3 | 3.8 | V | |
| Supply voltage differentials | V_{DD} | -0.25 | 0.25 | V | between any internally non-connected supply pins of the same kind, see Pin Configuration |
| DAC output current | I_O | -30 | | mA | for any single output |
| DAC output voltage | | -0.3 | $V_{DD}+0.3$ | mV | for any single output |
| RREF_I output current | I_O | -5 | | mA | for any single output |
| Total Power Dissipation | THD | | 1.8 | W | |
| ESD Protection | ESD | -2,0 | 2,0 | kV | MIL STD 883C method 3015.6, 100pF, 1500Ω (HBM) |
| ESD Protection | ESD | -1,5 | 1,5 | kV | EOS/ESD Assn. Standard DS 5.3-1993 (CDM) |
| | | | | | |
| Latch-Up Protection | | -100 | 100 | mA | all inputs/outputs |

All voltages listed are referenced to ground (0V, V_{SS}) except where noted.

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

6.2 Operating range

| Parameter | Symbol | Min | Nom | Max | Unit | Remark |
|-----------------------------|-----------|------|-----|----------------|------|----------------------------------------|
| Supply Voltages | V_{DD} | 3.15 | 3.3 | 3.45 | V | |
| Ambient Temperature | T_A | 0 | 25 | 70 | °C | |
| All TTL Inputs | | | | | | |
| High-Level Input Voltage | V_{IH} | 2.0V | | $V_{DD} + 0.2$ | V | |
| Low-Level Input Voltage | V_{IL} | -0.2 | | 0.8 | V | |
| Input Current | I_{IN} | | | +/- 5 | μA | |
| All TTL Outputs | | | | | | |
| High-Level Output Voltage | V_{OH} | 2.4 | | | V | $I_{OH} = -2.0$ mA |
| Low-Level Output Voltage | V_{OL} | | | 0.4 | V | $I_{OL} = 2.0$ mA |
| INPUT/OUTPUT: SDA | | | | | | |
| Low-Level Output Voltage | V_{OL} | | | 0.5 | V | at $I_{OL} = \text{max}$ |
| Clock TTL Input CLKM | | | | | | |
| Clock frequency | $1/T$ | | 27 | | MHz | see "Timing diagram clock" on page 183 |
| Low time | t_{WL} | 10 | | | ns | |
| High time | t_{WH} | 10 | | | ns | |
| Rise time | t_{TLH} | | | 10 | ns | |
| Fall time | t_{THL} | | | 10 | ns | |
| Input SYNCENM | | | | | | |
| Low time | t_{WL} | 22 | | | ns | see "Timing diagram clock" on page 183 |
| High time | t_{WH} | 22 | | | ns | |
| Rise time | t_{TLH} | | | 10 | ns | |
| Fall time | t_{THL} | | | 10 | ns | |
| Clock TTL Input CLKS | | | | | | |
| Clock frequency | $1/T$ | | 27 | | MHz | see "Timing diagram clock" on page 183 |
| Low time | t_{WL} | 10 | | | ns | |
| High time | t_{WH} | 10 | | | ns | |
| Rise time | t_{TLH} | | | 10 | ns | |
| Fall time | t_{THL} | | | 10 | ns | |

Electrical Characteristics

| Parameter | Symbol | Min | Nom | Max | Unit | Remark |
|-------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|-----|------|------|----------------------------------------------------------|
| Input SYNCENS | | | | | | |
| Low time | t_{WL} | 22 | | | ns | see "Timing diagram clock" on page 183 |
| High time | t_{WH} | 22 | | | ns | |
| Rise time | t_{TLH} | | | 10 | ns | |
| Fall time | t_{THL} | | | 10 | ns | |
| Clock TTL Input X1/CLKD | | | | | | |
| Clock frequency | $1/T$ | | 27 | | MHz | see "Timing diagram clock" on page 183 |
| Low time | t_{WL} | 10 | | | ns | |
| High time | t_{WH} | 10 | | | ns | |
| Rise time | t_{TLH} | | | 5 | ns | |
| Fall time | t_{THL} | | | 5 | ns | |
| I²C Bus (All Values Are Referred To min(V_{IH}) And max(V_{IL})), f_{SCL} = 400 KHz | | | | | | |
| High-Level Input Voltage | V _{IH} | 3 | | 5.25 | V | see "I ² C Bus timing START/STOP" on page 182 |
| Low-Level Input Voltage | V _{IL} | 0 | | 1.5 | V | see "I ² C Bus timing DATA" on page 182 |
| SCL Clock Frequency | f _{SCL} | 0 | | 400 | kHz | |
| Inactive Time Before Start Of Transmission | t _{BUF} | 1.3 | | | μs | |
| Set-Up Time Start Condition | t _{SU;STA} | 0.6 | | | μs | |
| Hold Time Start Condition | t _{HD;STA} | 0.6 | | | μs | |
| SCL Low Time | t _{LOW} | 1.3 | | | μs | |
| SCL High Time | t _{HIGH} | 0.6 | | | μs | |
| Set-Up Time DATA | t _{SU;DAT} | 100 | | | ns | |
| Hold Time DATA | t _{HD;DAT} | 0 | | | μs | |
| SDA/SCL Rise Times | t _R | | | 300 | ns | |
| SDA/SCL Fall Times | t _F | | | 300 | ns | |
| Set-Up Time Stop Condition | t _{SU;STO} | 0.6 | | | μs | |
| Output valid from clock | t _{AA} | | | 900 | ns | |
| Input filter spike suppression (SDA and SCL pins) | t _{SP} | | | 50 | ns | |
| Low-Level Output Current | I _{OL} | | | 3 | mA | |

Electrical Characteristics

| Parameter | Symbol | Min | Nom | Max | Unit | Remark |
|----------------------------------------|-----------|------|------|------|----------|-----------------------------------------|
| Inputs crystal connections X1/CLKD, X2 | | | | | | see "Clock circuit diagram" on page 183 |
| Crystal frequency | X_{tal} | | 27.0 | | MHz | fundamental crystal |
| Equivalent parallel Capacitance | C_{in} | | | 27 | pF | |
| Equivalent parallel Capacitance | C_{out} | | | 27 | pF | |
| Resonance impedance | ZR | | 40 | | Ω | |
| Digital-To-Analog-Conversion | | | | | | |
| DAC sample rate | f_s | 4.5 | 54.0 | 60 | MHz | |
| RREF_I output current | I_{ref} | -1.3 | -1.9 | -2.5 | mA | |
| UREF_I input voltage | U_{ref} | 0.8 | 0.9 | 1.0 | V | |

6.3 Characteristics (Under operating range conditions)

| Parameter | Symbol | Min | Max | Unit | Remark |
|-----------------------------------------------------------------|----------|--------|--------|---------|----------------------------------------|
| Average Supply Current | | t.b.d. | t.b.d. | mA | All V_{DD} pins, typ. t.b.d.mA |
| All Digital Inputs (Including I/O Inputs) | | | | | |
| Input Capacitance | | | 10 | pF | |
| Input Leakage Current | | -5 | 5 | μ A | |
| TTL Inputs: YINM, UVINM, HINM, VINM (Referenced To CLKM) | | | | | |
| Set-Up Time | t_{SU} | 7 | | ns | see "Timing diagram clock" on page 183 |
| Input Hold Time | t_{IH} | 6 | | ns | |
| TTL Inputs: YINS, UVINS, HINS, VINS (Referenced To CLKS) | | | | | |
| Set-Up Time | t_{SU} | 7 | | ns | see "Timing diagram clock" on page 183 |
| Input Hold Time | t_{IH} | 6 | | ns | |
| TTL Outputs: HOUT, VOUT, BLANK (Referenced To CLKOUT) | | | | | |
| Hold time | t_{OH} | 6 | | ns | see "Timing diagram clock" on page 183 |
| Delay time | t_{OD} | | 25 | ns | CL = 50 pF, 27 MHz |
| TTL Inputs: SYNCENM (Referenced To CLKM) | | | | | |
| Set-Up Time | t_{SU} | 25 | | ns | see "Timing diagram clock" on page 183 |
| Input Hold Time | t_{IH} | 0 | | ns | |
| TTL Inputs: SYNCENS (Referenced To CLKS) | | | | | |
| Set-Up Time | t_{SU} | 25 | | ns | see "Timing diagram clock" on page 183 |

Electrical Characteristics

| | | | | | |
|--------------------------------------------------------------------------------------|--------------|--------|-------|------------------|------------------------------------------------------|
| Input Hold Time | t_{IH} | 0 | | ns | |
| Digital-To-Analog Conversion (9 bit): Current Source Outputs IY_O, IU_O, IV_O | | | | | |
| Full range output current | I_{OFR} | -19 | -17 | mA | $U_{ref}=typ., T_A=nom., I_{REF}=typ., R_L=75\Omega$ |
| Full range output matching | DDLOUT | -3% | 3% | | DAC output U and V to each other |
| Full range output accuracy | DLOUT | -3% | 3% | | within operating range |
| Current source output resistance | R_O | 20 | | k Ω | $U_{ref}=nom., T_A=nom., I_{REF}=nom.$ |
| Supply voltage dependency of I_{OFR} | dI/dV_{DD} | -0.015 | 0.015 | mA/V | $U_{ref}=nom., T_A=nom., I_{REF}=nom., R_L=75\Omega$ |
| Temperature dependency of I_{OFR} | dI_{OFR} | -10 | 10 | $\mu A/^\circ C$ | $U_{ref}=nom., I_{REF}=nom., R_L=75\Omega$ |
| Full range output voltage | V_O | | 1.5 | V | $U_{ref}=nom., T_A=nom., I_{REF}=nom.$ |
| DC differential non-linearity | DNL | -1 | 1 | LSB | |
| DC differential integral non-linearity | INL | -2 | 2 | LSB | |
| DAC Reference Pins: UREF_I, RREF_I (analog) | | | | | |
| Offset voltage between UREF_I and RREF_I | U_{OFFSET} | -40 | 40 | mV | |
| UREF_I input current | I_{UREF} | -10 | 10 | μA | |

Application information

7 Application information

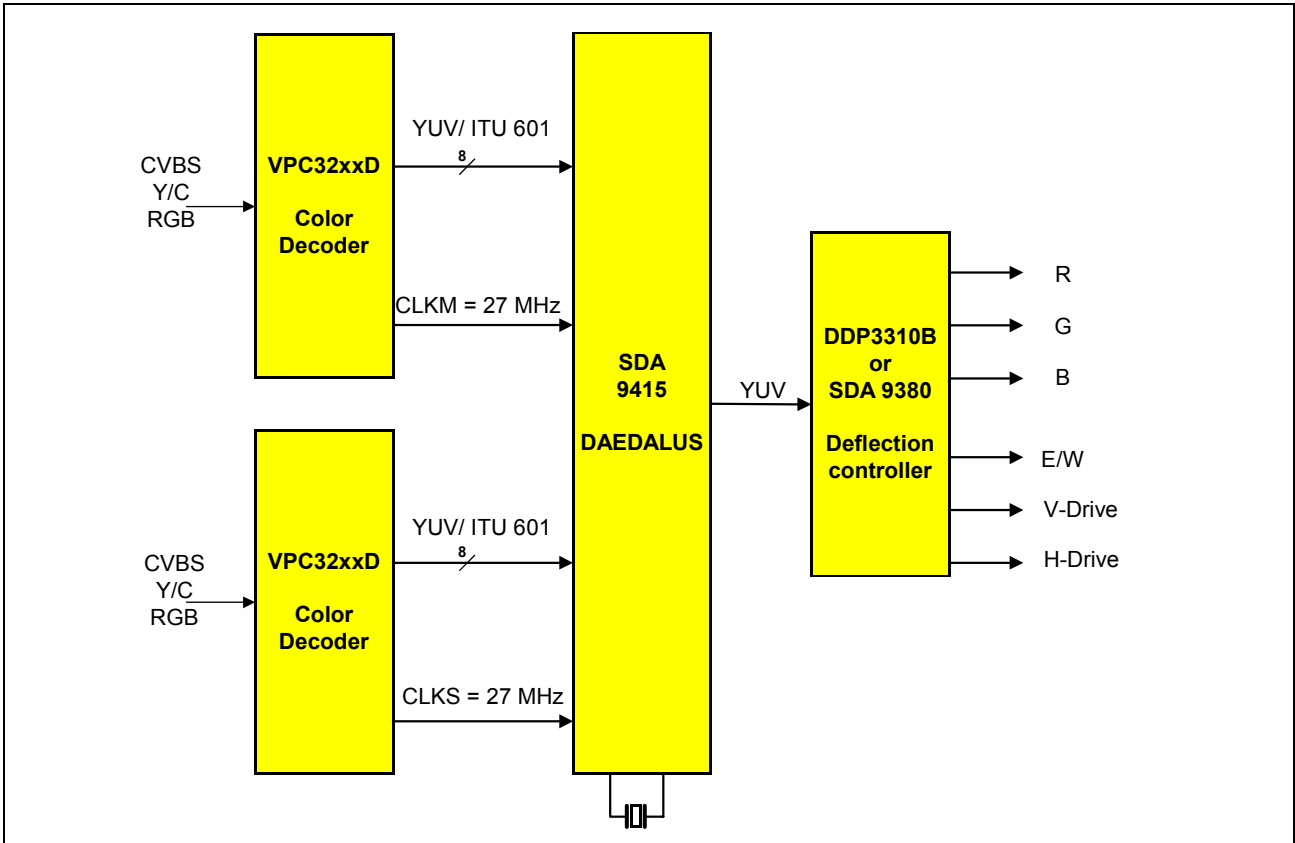
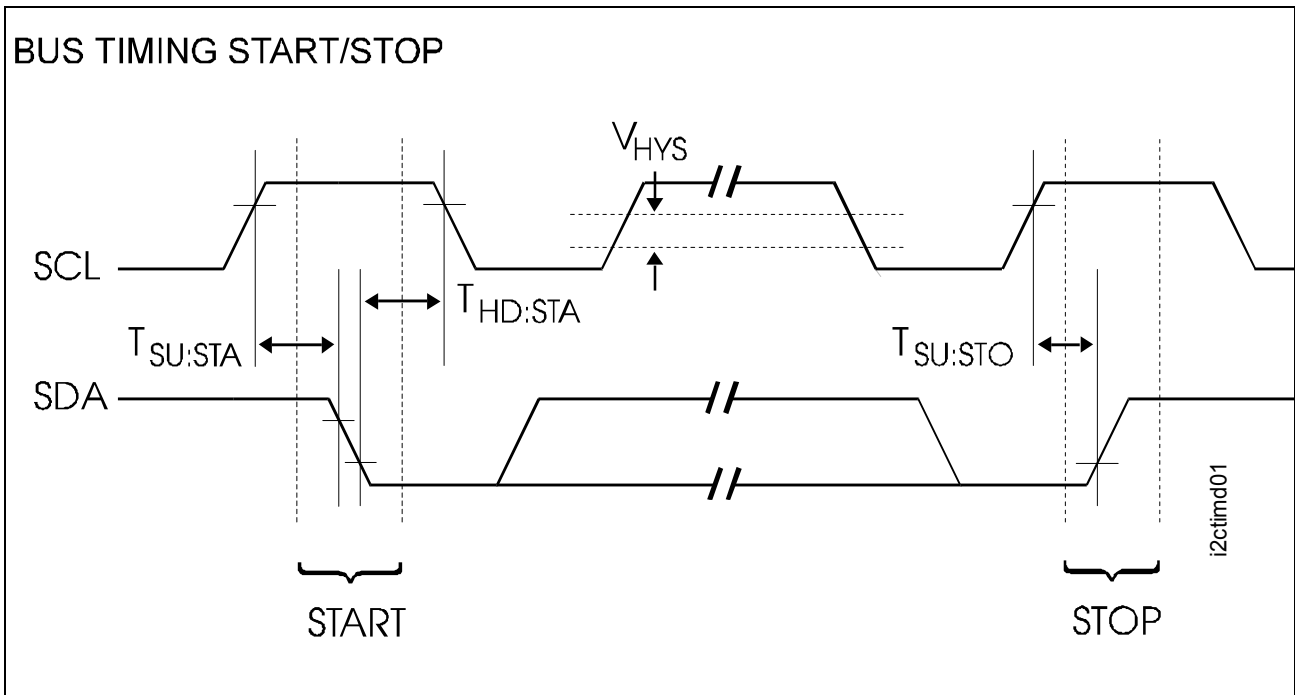


Figure 55 Application for SDA 9415

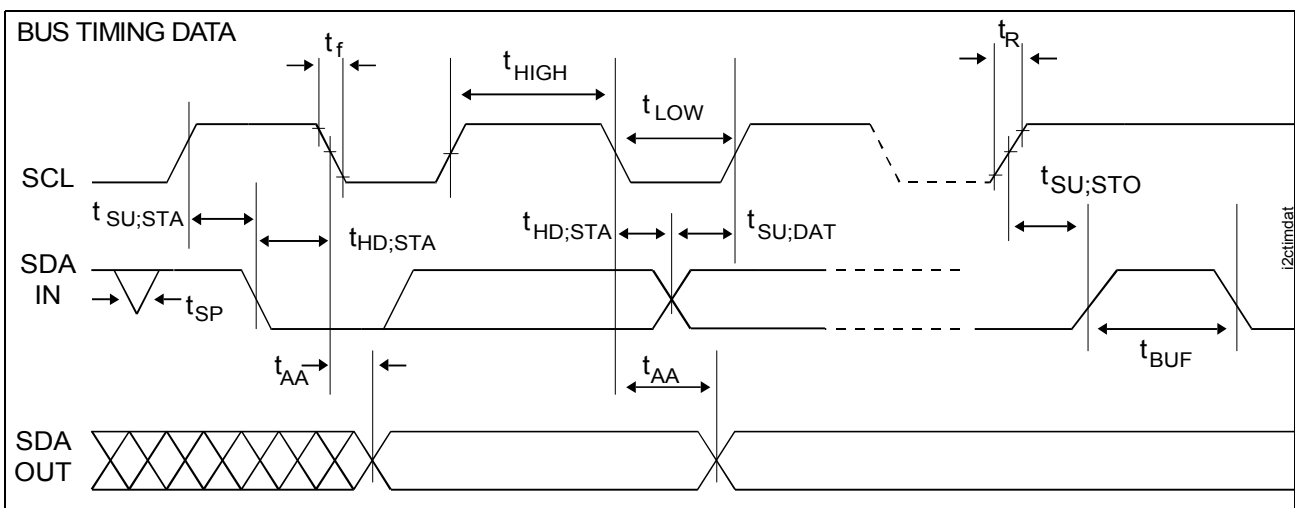
Wave forms

8 Wave forms

8.1 I²C Bus timing START/STOP

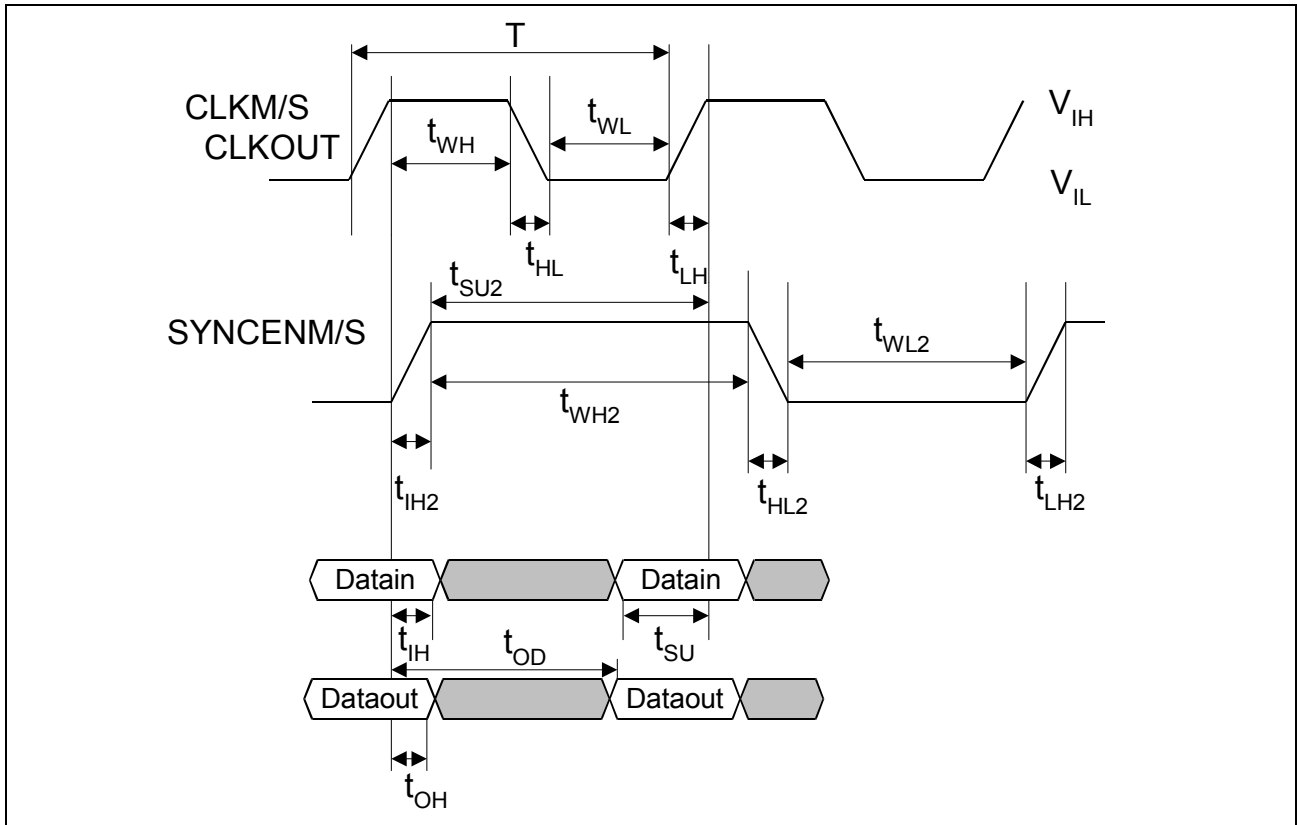


8.2 I²C Bus timing DATA

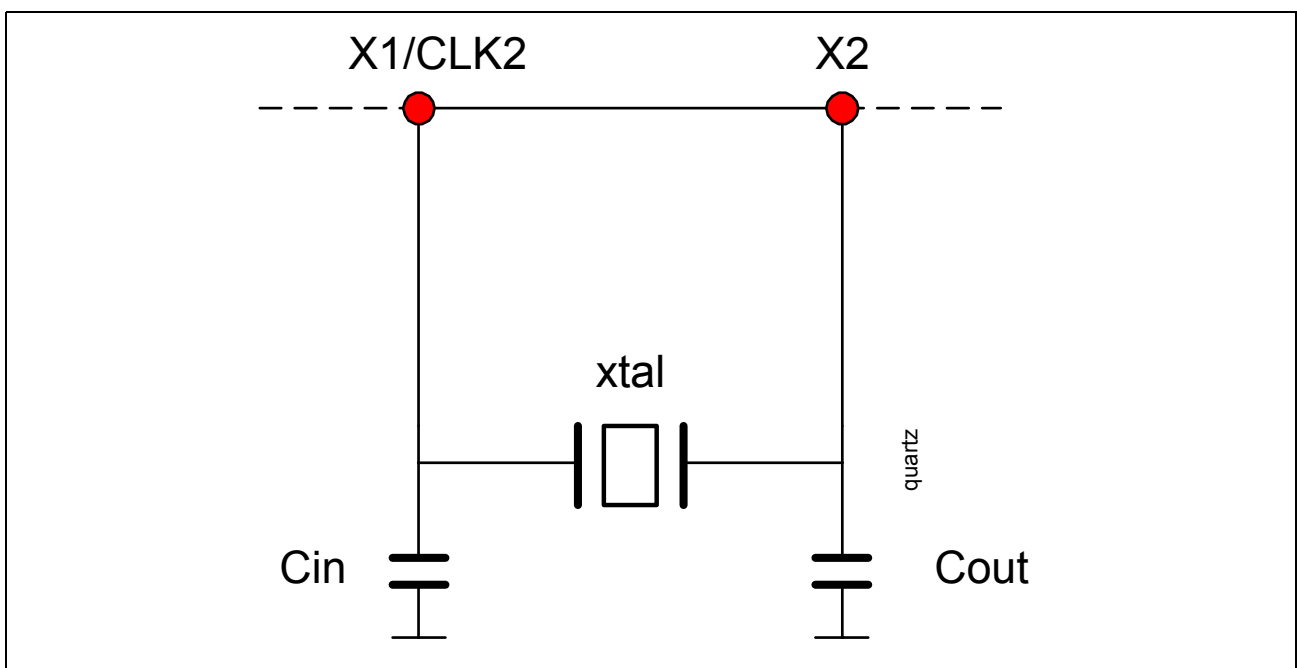


Wave forms

8.3 Timing diagram clock



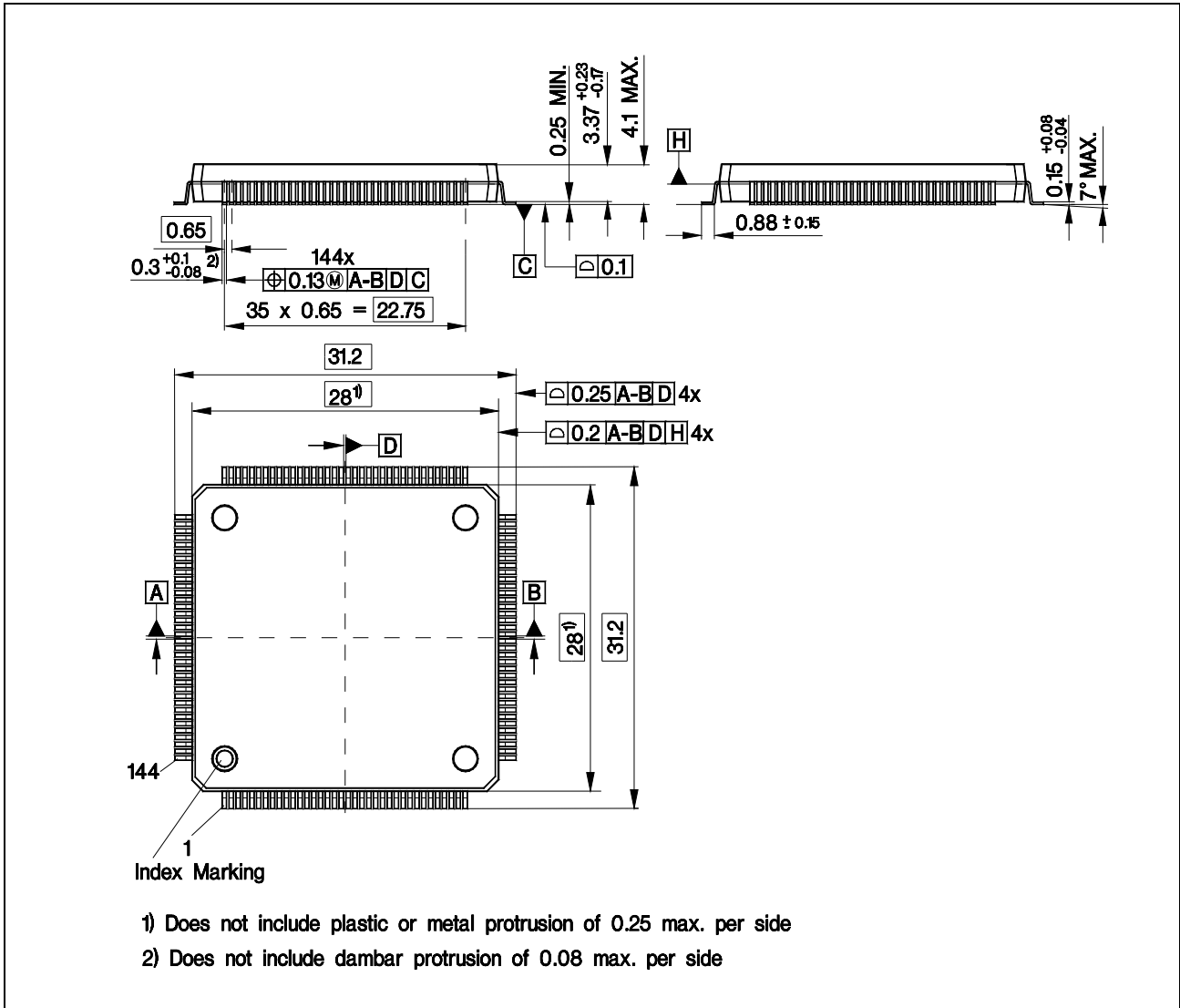
8.4 Clock circuit diagram



Package Outlines

9 Package Outlines

P-MQFP-144-2



[all dimensions in mm]

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Printed in Germany
Order No. 6251-560-1PD

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